MX25V5126F

2.3V-3.6V, 512K-BIT [x 1/x 2]
CMOS SERIAL NOR FLASH

Key Features

- *Voltlage Range VCC: 2.3V - 3.6V*
- *Dual I/O Supported*
- *Unique ID*
- *Support conditional accelerated tBE and tCE*
- *Enhanced Program and Erase performance (for increased factory production throughput)*

Contents

2.3V-3.6V 512K-BIT [x 1/x 2] CMOS SERIAL FLASH

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface - Mode 0 and Mode 3
- 524,288 x 1 bit structure or 262,144 x 2 bits (Dual Output mode) Structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K/64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.3 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast Read:
  - 1 I/O:
    80MHz with 8 dummy cycles (2.7V-3.6V)
    50MHz with 8 dummy cycles (2.3V-2.7V)
  - 2 I/O:
    80MHz with 4 dummy cycles (2.7V-3.6V)
    50MHz with 4 dummy cycles (2.3V-2.7V)
  - Fast program time: 1.6ms /page (256-byte)
  - Byte program time: 20us
  - Fast erase time:
    50ms(typ.)/sector (4K-byte per sector);
    0.3s(typ.)/block (32K-byte per block);
    0.6s(typ.)/block (64K-byte per block);
    1.8s(typ.)/chip.

- Low Power Consumption
  - Low active read current: 6mA(max.) at 50MHz
  - Low active programming current: 5mA (typ.)/page
  - Low active sector erase current: 5mA (typ.)
  - Low standby current: 5uA (typ.)
  - Deep power-down mode: 1uA (typ.)

- Minimum 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format: 1-byte Command code
- Block Lock protection: The BP0-BP3 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 2-byte Device ID
  - RES command, 1-byte Device ID
- Support Unique ID (Please contact local Macronix sales for detail information)

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Output for Dual output mode
- SO/SIO1
  - Serial Data Output or Serial Data Output for Dual output mode
- WP# pin
  - Hardware write protection
- **PACKAGE**
  - 8-USON (2x3mm)
  - 8-pin TSSOP (173mil)
  - 8-pin SOP (150mil)

All devices are RoHS compliant and Halogen-free

2. GENERAL DESCRIPTION

MX25V5126F is a CMOS 512Kb bits Serial NOR Flash memory, which is configured as 65,536 x 8 internally. MX25V5126F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25V5126F provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis. Erase command is executed on chip or on 4K-byte sector, or 32KB block (32K-byte), or 64K-byte block, or whole chip basis.

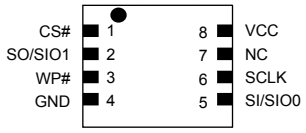
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

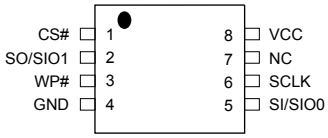
The MX25V5126F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

3. PIN CONFIGURATIONS

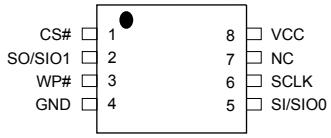
8-LAND USON (2x3mm)



8-PIN TSSOP (173mil)



8-PIN SOP (150mil)

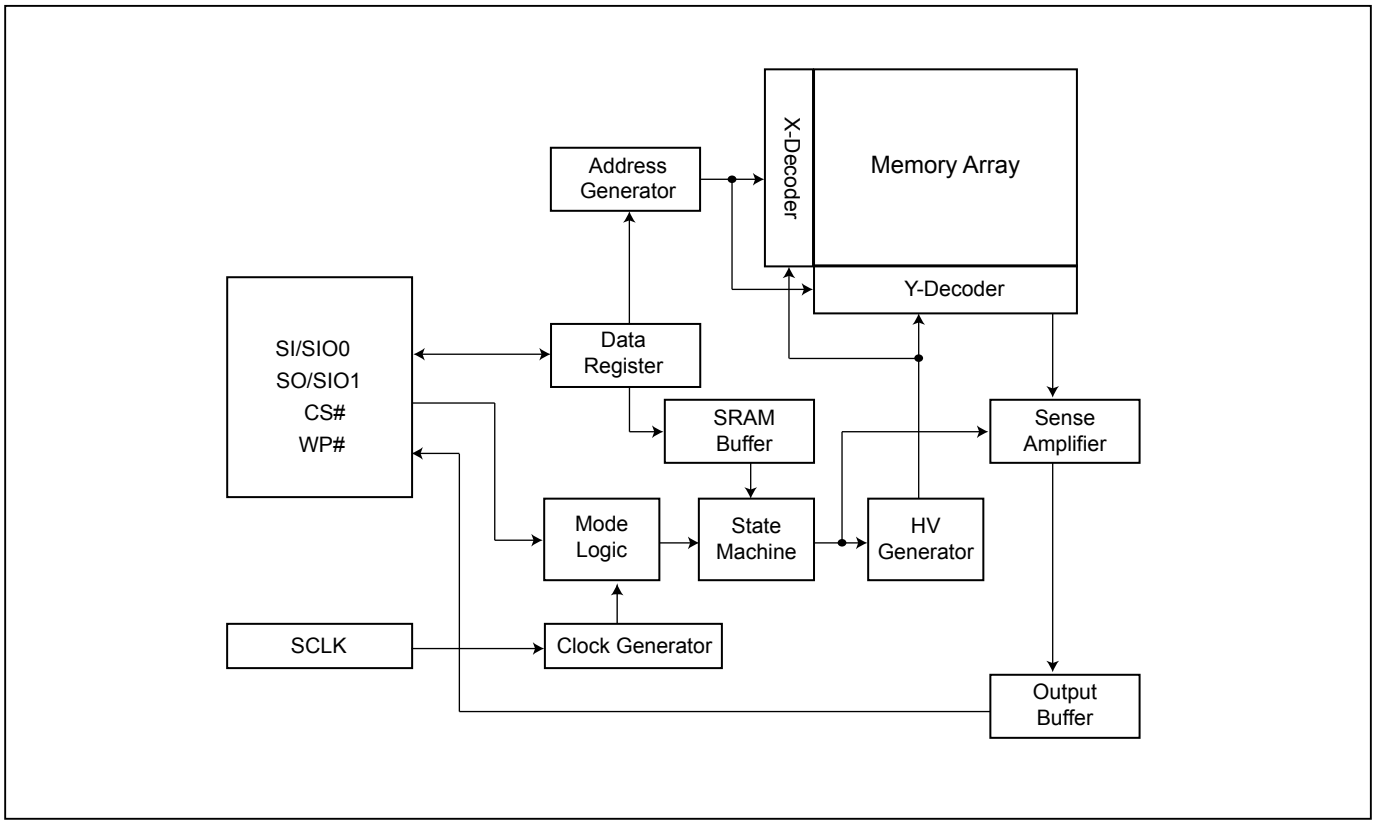


4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for Dual output mode)
SCLK	Clock Input
WP#	Write Protection
VCC	+ 3.3V Power Supply
GND	Ground

Note: *The pin of WP# will remain internal pull up function while this pin is not physically connected in system configuration.*
However, the internal pull up function will be disabled if the system has physical connection to WP# pin.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- **Valid command length checking:** The command length will be checked whether it is at byte base and completed on byte boundary.
- **Write Enable (WREN) command:** WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- **Deep Power Down Mode:** By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power-down mode command (RDP), Read Electronic Signature command (RES), power-cycle, or reset. For more details, please refer to *"9-18. Deep Power-down (DP)"* section.
- **Protection Features:** There are some protection features that could protect content change from unintentional write and hostile access:
  - **A. The software Protection Mode (SPM) -** Use BP0, BP1, BP3 bits to set the part of memory to be protected as read only The definition of protect area is shown as *"Table 1. Protected Area Sizes"*.
  - **B. Hardware Protection Mode (HPM) -** use WP# by setting WP# going low to protect the BP0, BP1, BP3 bits and status register write protection (SRWD).

Table 1. Protected Area Sizes

Status bit				Protect level	512Kb
BP3	BP2	BP1	BP0		
0	X	0	0	0 (none)	None
0	X	0	1	1 (1 block)	All
0	X	1	0	2 (1 block)	All
0	X	1	1	3 (1 block)	All
1	X	0	0	0 (none)	None
1	X	0	1	1 (1 block)	All
1	X	1	0	2 (1 block)	All
1	X	1	1	3 (1 block)	All

Note: X means “Don’t Care”

7. MEMORY ORGANIZATION

Table 2. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
0	1	15	00F000h	00FFFFh
		:	:	:
		3	003000h	003FFFh
	|	2	002000h	002FFFh
		1	001000h	001FFFh
	0	0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure the device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

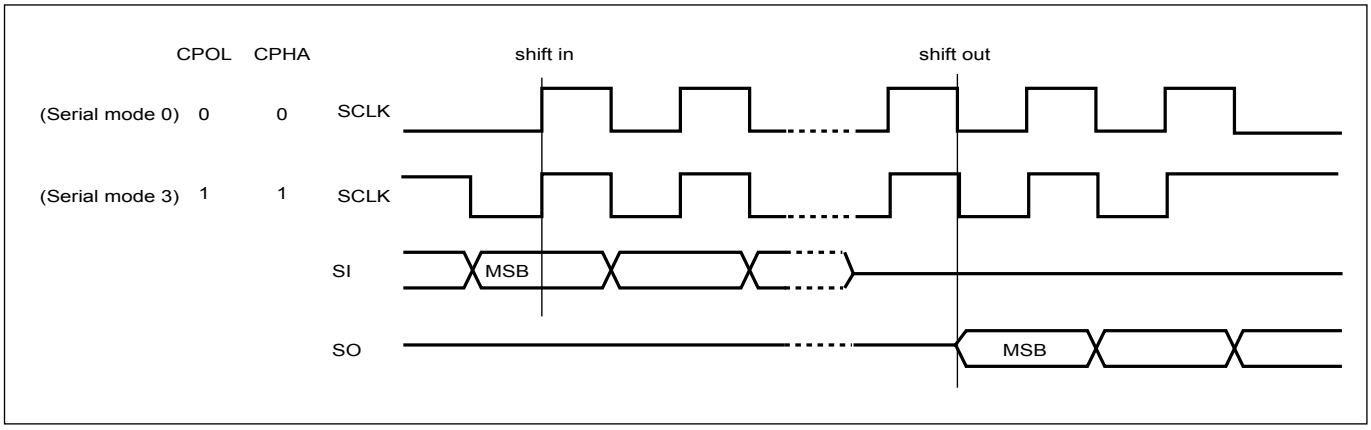
3. When correct command is inputted to this device, it enters active mode and stay in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, READ, FAST_READ, DREAD, RES and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP, DP, RSTEN and RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, and Erase.

Figure 1. Serial Modes Supported



Note: *CPOL indicates clock polarity of Serial master:*
-CPOL=1 for SCLK high while idle,
-CPOL=0 for SCLK low while not transmitting.
CPHA indicates clock phase.
The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

9. Timing Analysis

Figure 2. Serial Input Timing

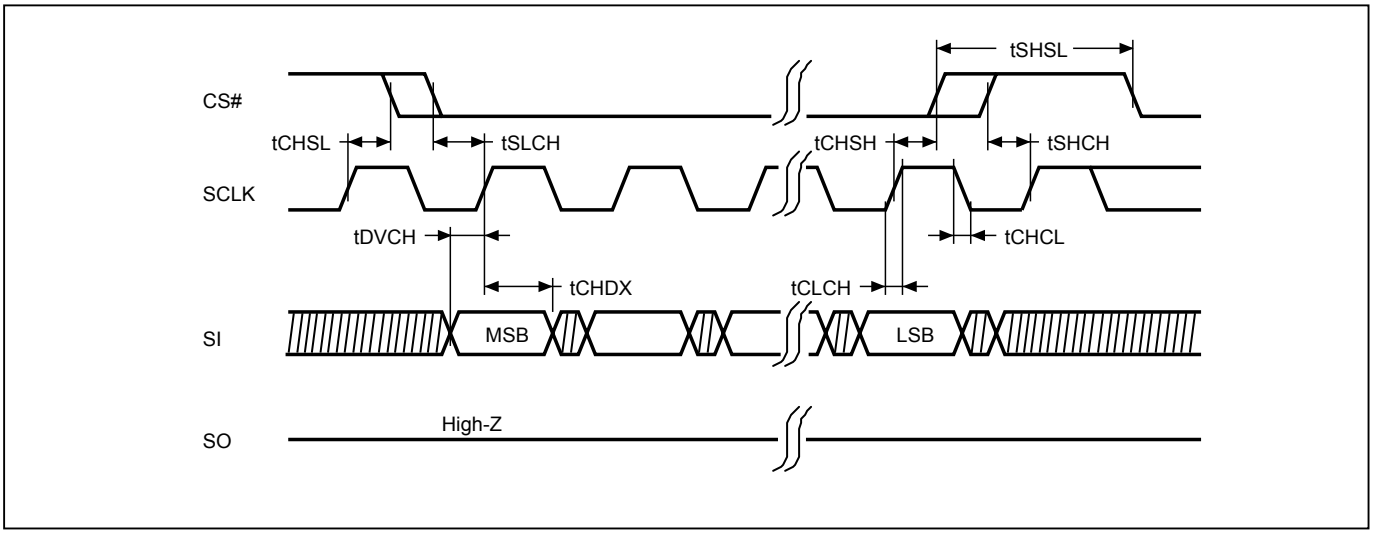


Figure 3. Output Timing

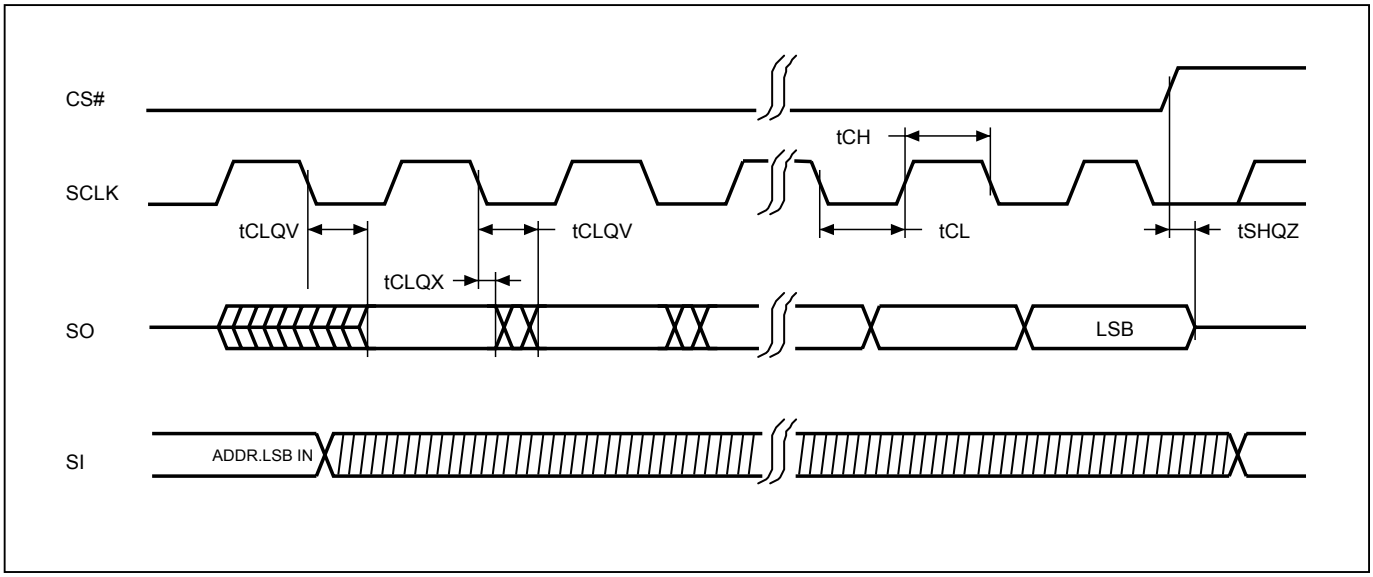


Table 3. COMMAND DESCRIPTION

	COMMAND (byte)	I/O	1st byte	2nd byte	3rd byte	4th byte	5th byte	Action
Read/Write Array	**READ (Normal Read)**	1	03 (hex)	ADD1	ADD2	ADD3		n bytes read out until CS# goes high
	Fast Read (Fast Read Data)	1	0B (hex)	ADD1	ADD2	ADD3	Dummy	n bytes read out until CS# goes high
	DREAD (1 x I / 2O Read Command)	2	3B (hex)	ADD1	ADD2	ADD3	Dummy	n bytes read out by Dual Output until CS# goes high
	2READ (2 x I/O Read Command)	2	BB (hex)	ADD1	ADD2	ADD3	Dummy	n bytes read out by 2 x I/O until CS# goes high
	SE (Sector Erase)	1	20 (hex)	ADD1	ADD2	ADD3		Erase the selected sector
	BE 32K (Block Erase 32KB)	1	52 (hex)	ADD1	ADD2	ADD3		Erase the selected 32KB block
	BE (Block Erase 64KB)	1	D8 (hex)	ADD1	ADD2	ADD3		Erase the selected 64KB block
	CE (Chip Erase)	1	60 or C7 (hex)					Erase the whole chip
	PP (Page Program)	1	02 (hex)	ADD1	ADD2	ADD3		Program the selected page
Register/ Setting	**WREN (Write Enable)**	1	06 (hex)					Set the (WEL) write enable latch bit
	WRDI (Write Disable)	1	04 (hex)					Reset the (WEL) write enable latch bit
	FMEN (Factory mode enable)	1	41 (hex)					Enable factory mode
	RDSR (Read Status Register)	1	05 (hex)					Read out the status register
	WRSR (Write Status Register)	1	01 (hex)					Write new values to the status register
	DP (Deep Power- down)	1	B9 (hex)					Enter deep power down mode
	RDP (Release from deep power down)	1	AB (hex)					release from deep power down mode
ID/Reset	**RDID (Read Identification)**	1	9F (hex)					Output manufacturer ID and 2-byte device ID
	RES (Read Electronic ID)	1	AB (hex)	x	x	x		Read out 1-byte Device ID
	REMS (Read Electronic Manufacturer & Device ID)	1	90 (hex)	x	x	ADD *(Note 1)*		Output the manufacturer ID and device ID
	RSTEN (Reset Enable)	1	66 (hex)					
	RST (Reset Memory)	1	99 (hex)					*(Note 3)*

Notes:

1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.
2) It is not recommended to adopt any other code which is not in the command definition table above.
3) The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

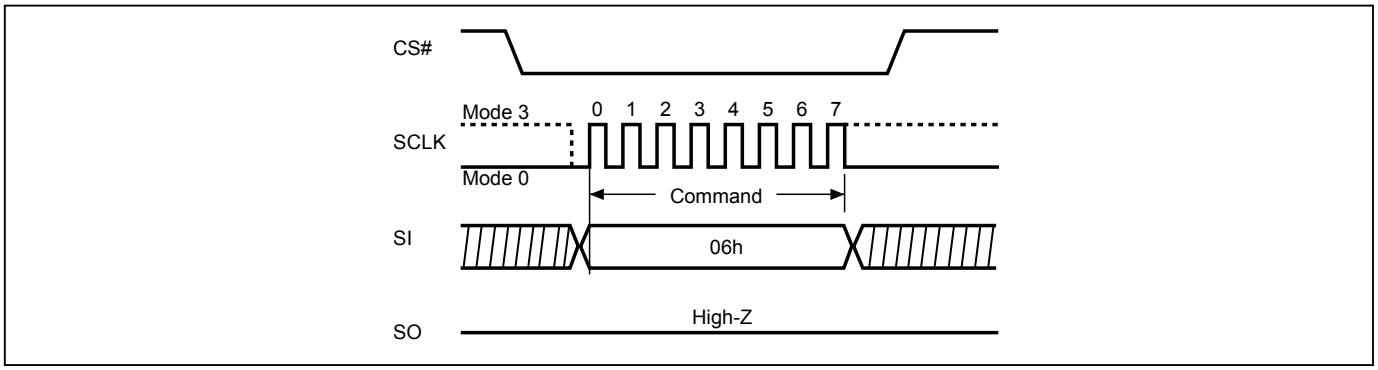
9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→send WREN instruction code→ CS# goes high.

The SIO[1:0] are "don't care" .

Figure 4. Write Enable (WREN) Sequence



9-2. Write Disable (WRDI)

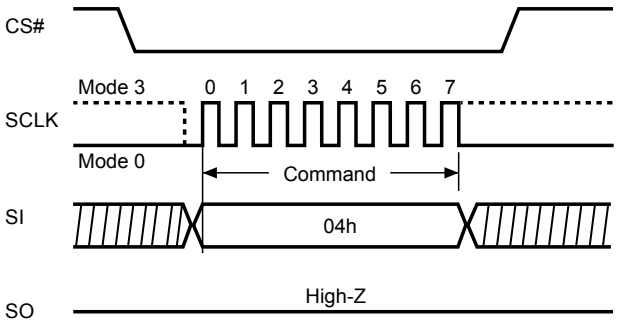
The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→send WRDI instruction code→CS# goes high.

The SIO[1:0] are "don't care".

The WEL bit is reset by following situations:
- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Completion of Softreset (RSTEN & RST) instruction

Figure 5. Write Disable (WRDI) Sequence



9-3. Factory Mode Enable (FMEN)

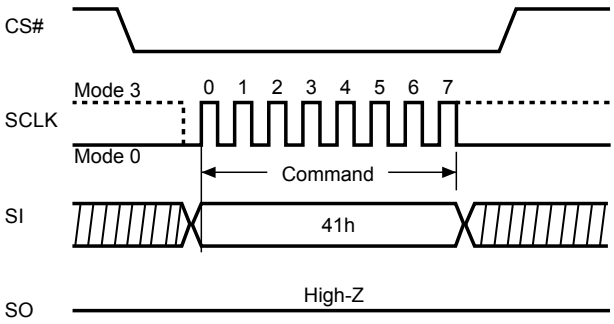
The Factory Mode Enable (FMEN) instruction is for enhance Program and Erase performance for increase factory production throughput. The FMEN instruction need to combine with the instructions which are intended to change the device content, like PP, SE, BE32K, BE, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→sending FMEN instruction code→ CS# goes high. A valid factory mode operation need to included three sequences: WREN instruction → FMEN instruction→ Program or Erase instruction.

The FMEN is reset by following situations

- Power-up
- PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- Softreset command completion

Figure 6. Factory Mode Enable (FMEN) Sequence



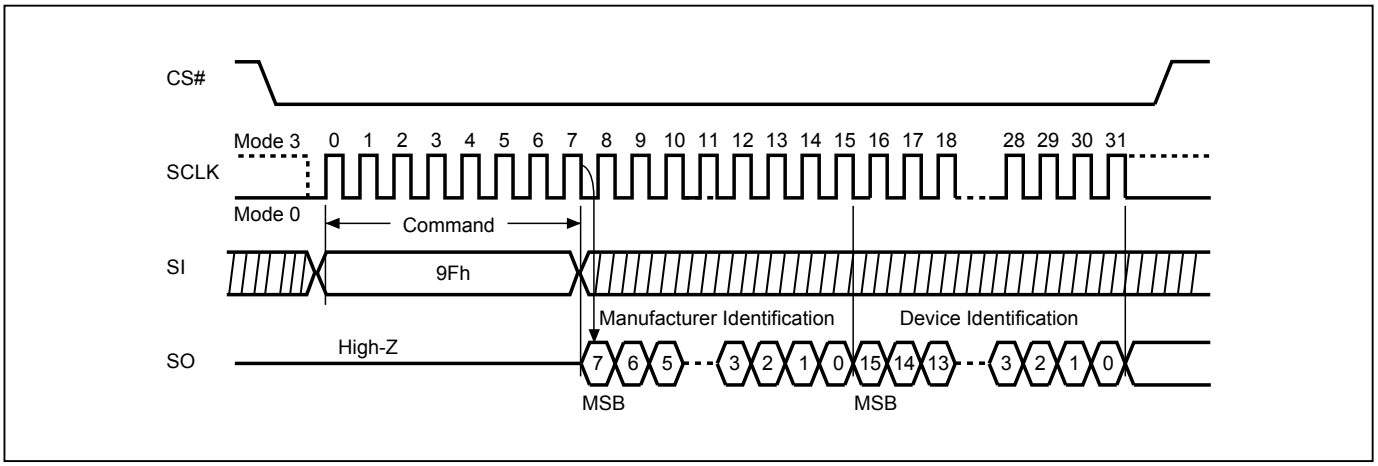
9-4. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 4. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ send RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 7. Read Identification (RDID) Sequence

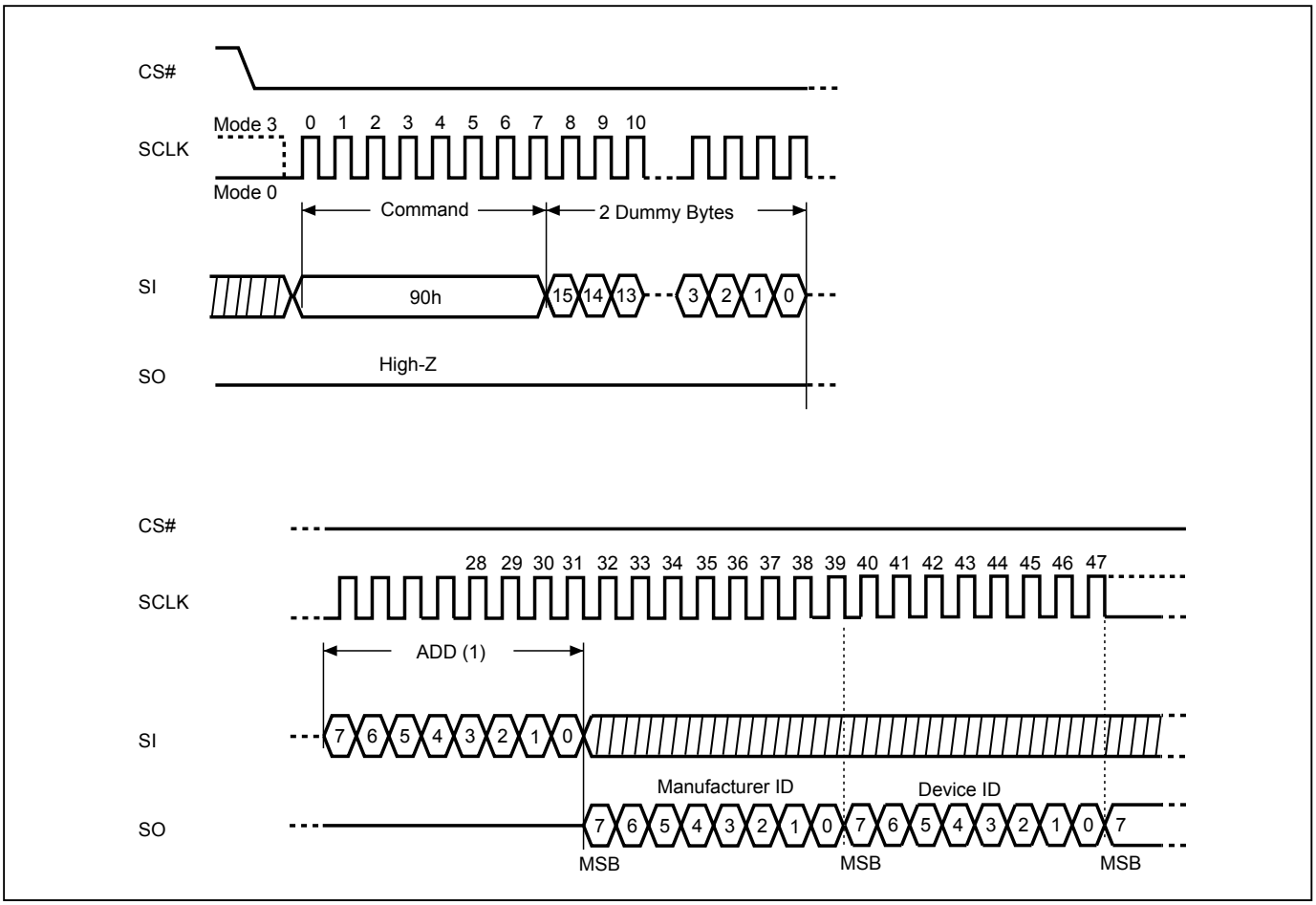


9-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 4. ID Definitions"*.

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 8. Read Electronic Manufacturer & Device ID (REMS) Sequence



Note: (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

9-6. ID Read

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issuing RDID instruction is: CS# goes low→ send RDID instruction code→24-bits ID data out on SO→ to end RDID operation, drive CS# to high at any time during data out.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Table 4. ID Definitions

Command Type	Command Code	MX25V5126F		
RDID	9Fh	Manufacturer ID	Memory Type	Memory Density
		C2	20	10
RES	ABh	Electronic ID		
		05		
REMS	90h	Manufacturer ID	Device ID	
		C2	05	

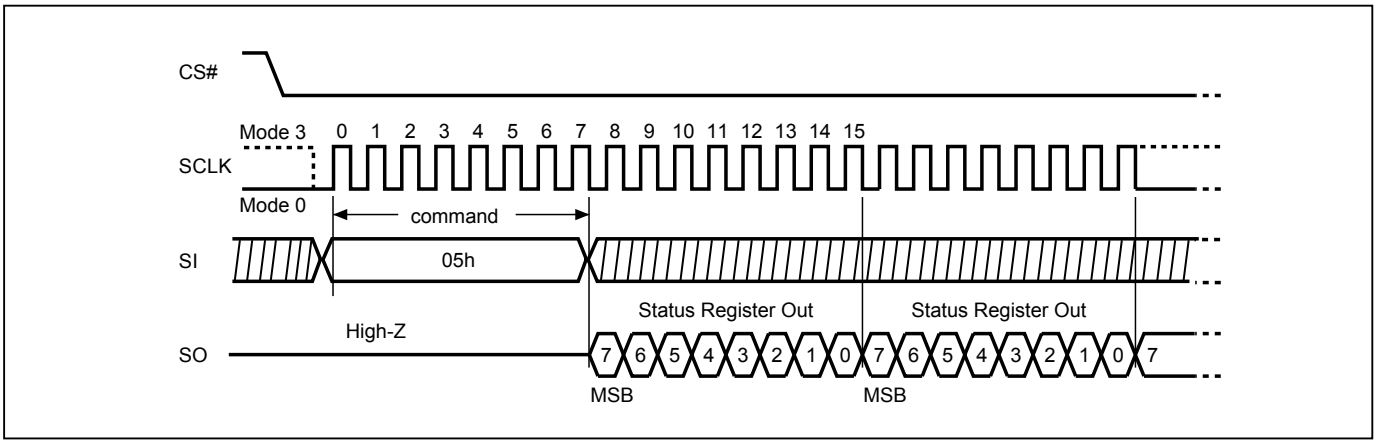
9-7. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ Send RDSR instruction code→ Status Register data out on SO.

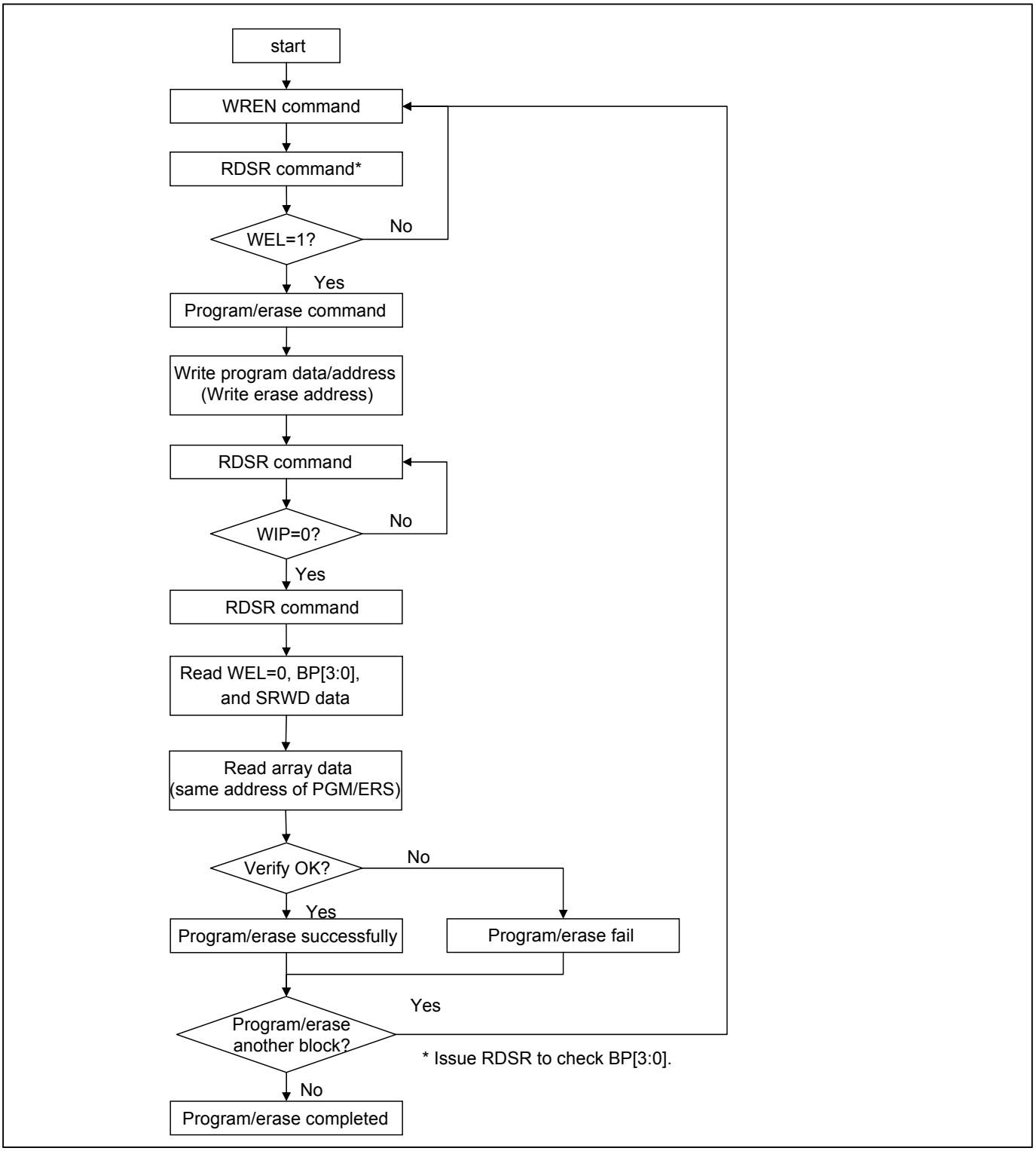
The SIO[1:0] are "don't care".

Figure 9. Read Status Register (RDSR) Sequence



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 10. Program/Erase flow with read array data



Status Register

The definitions of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to "1" by the WREN instruction. WEL needs to be set to "1" before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to "0" when a program or erase operation completes. To ensure that both WIP and WEL are "0" and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be "0" before checking that WEL is also "0". If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to "0".

BP3, BP1, BP0 bits. The Block Protect (BP3, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 1. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0 or BP3, BP2, BP1, BP0 are set to "1,X,0,0", the CE instruction can be executed).

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP1, BP0) are read only.

Table 5. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	Reserved	BP3 (level of protected block)	Reserved	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	Reserved	*(Note 1)*	Reserved	*(Note 1)*	*(Note 1)*	1=write enabled 0=not write enabled	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note: *1. Please refer to "Table 1. Protected Area Sizes".*

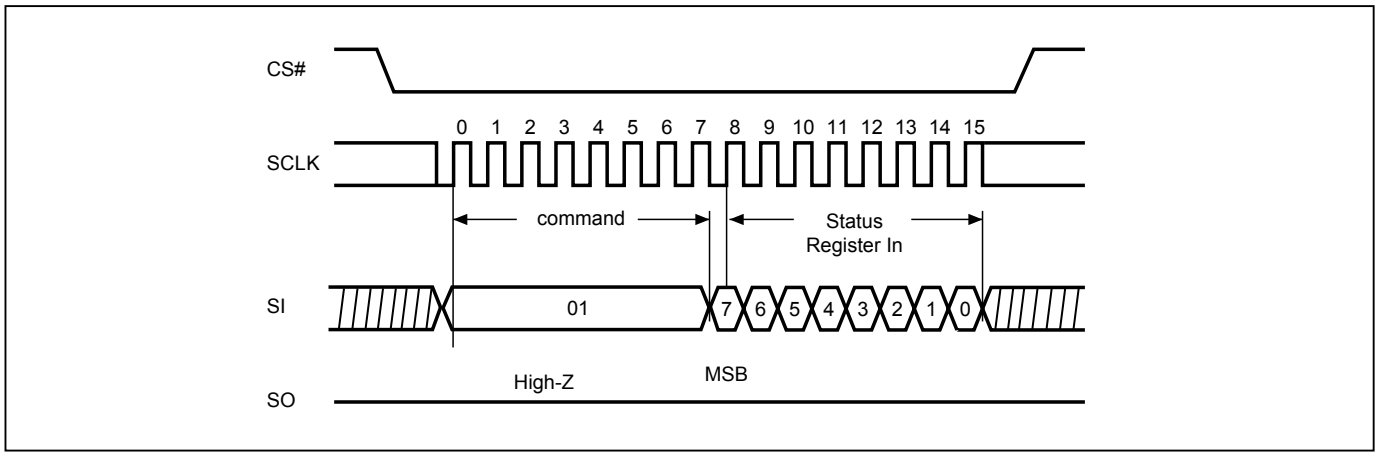
9-8. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 8. AC CHARACTERISTICS"*.) The WRSR can also set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ send WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 11. Write Status Register (WRSR) Sequence



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP1, BP0. The protected area, which is defined by BP3, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP1, BP0. The protected area, which is defined by BP3, BP1, BP0, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note:

To exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP1, BP0.

Table 6. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP1, BP0) bits of the Status Register, as shown in the table above.

Figure 12. WRSR Flow

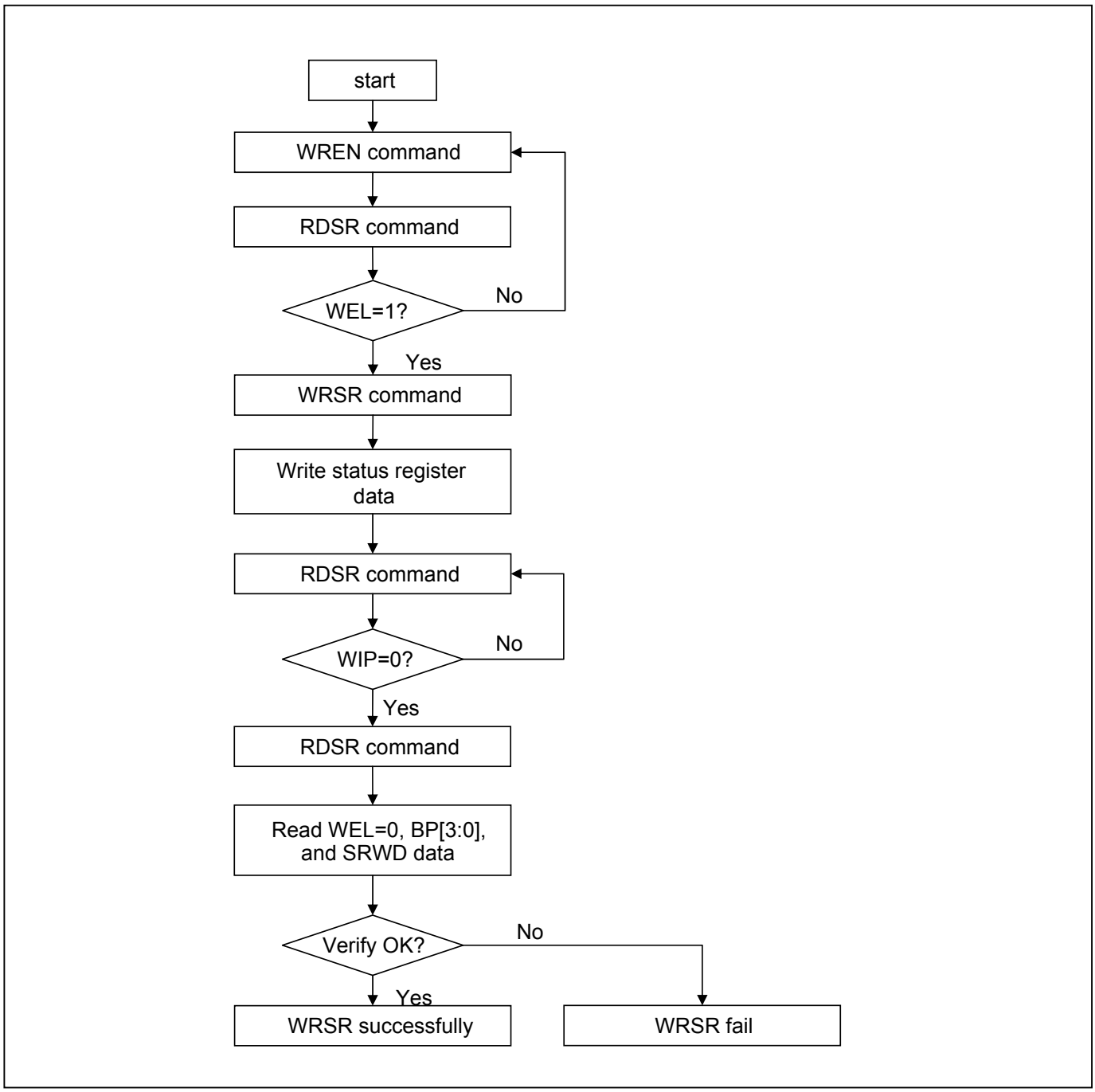
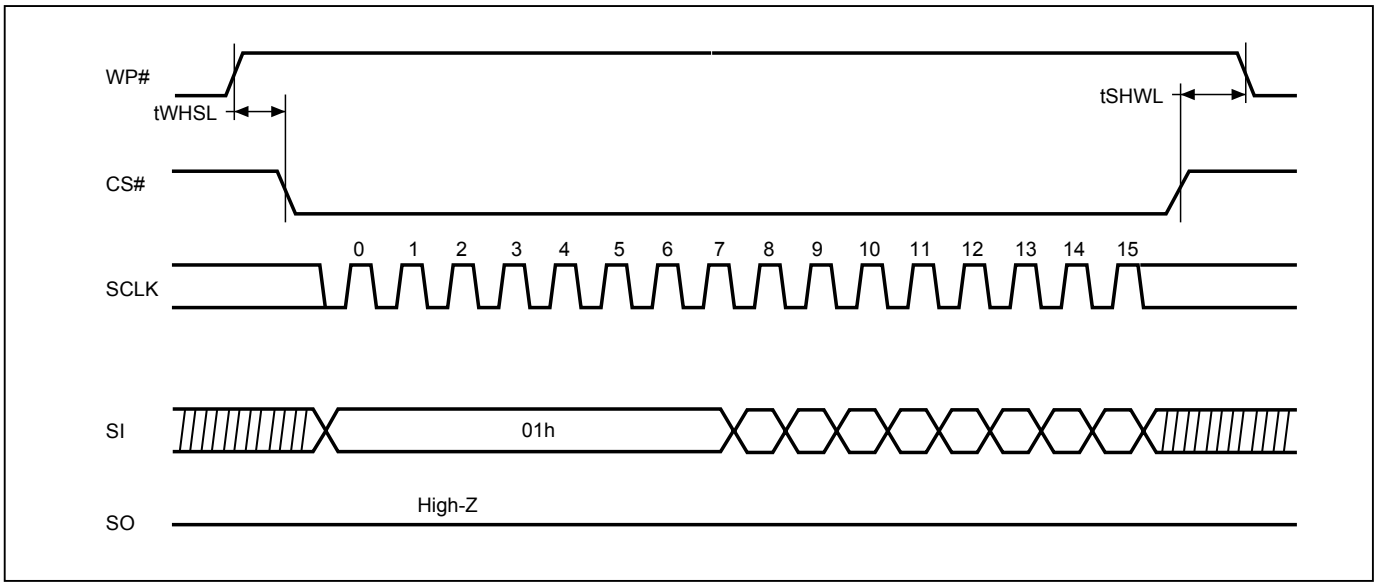


Figure 13. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



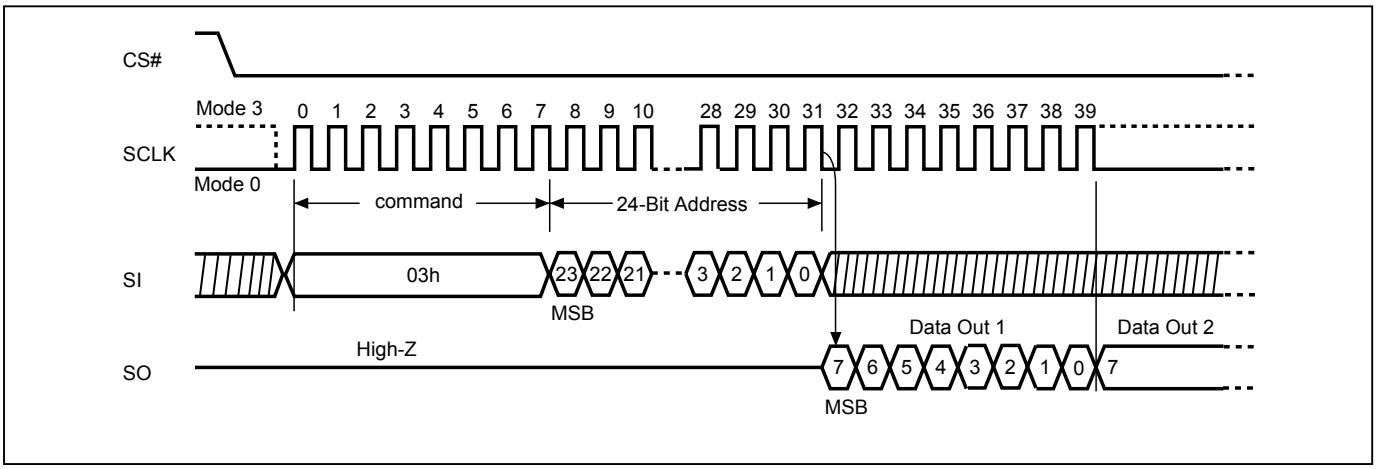
Note: WP# must be kept high until the embedded operation finish.

9-9. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→send READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 14. Read Data Bytes (READ) Sequence



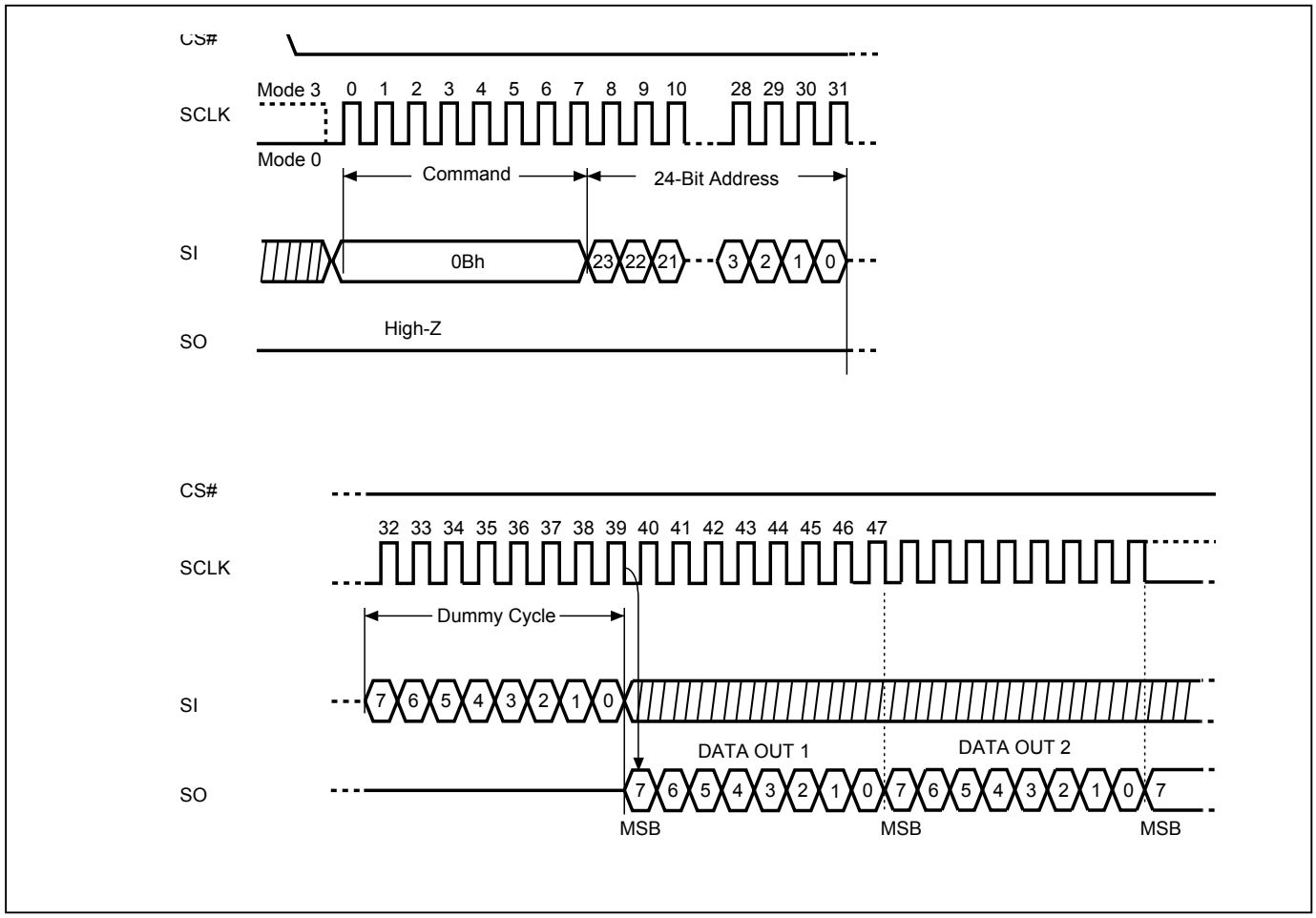
9-10. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ send FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 15. Read at Higher Speed (FAST_READ) Sequence



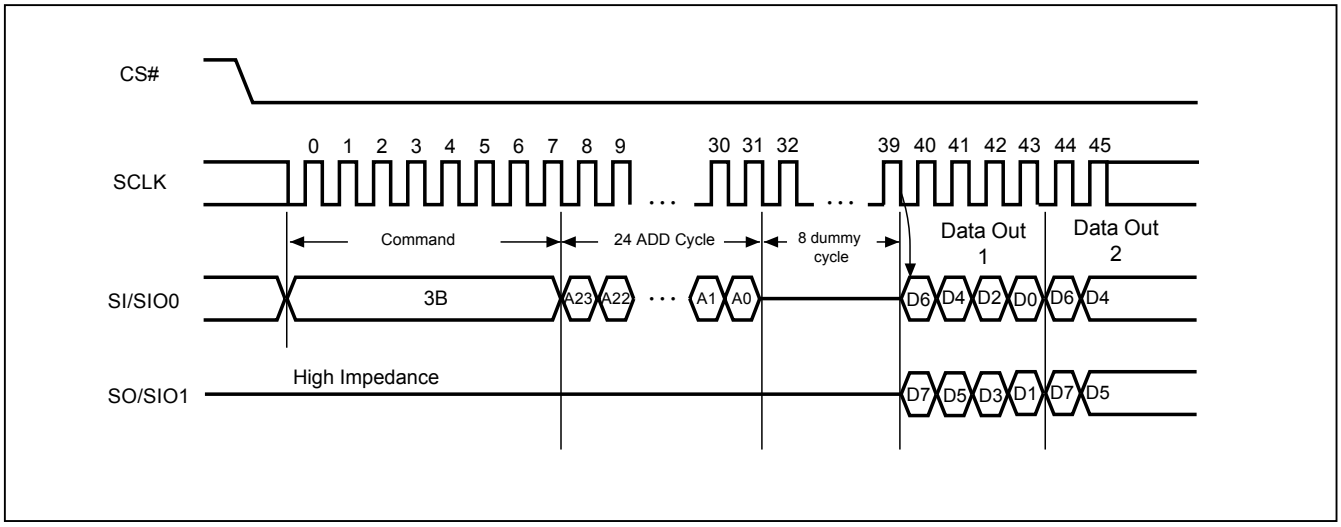
9-11. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → send DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 16. Dual Read Mode Sequence (Command 3Bh)



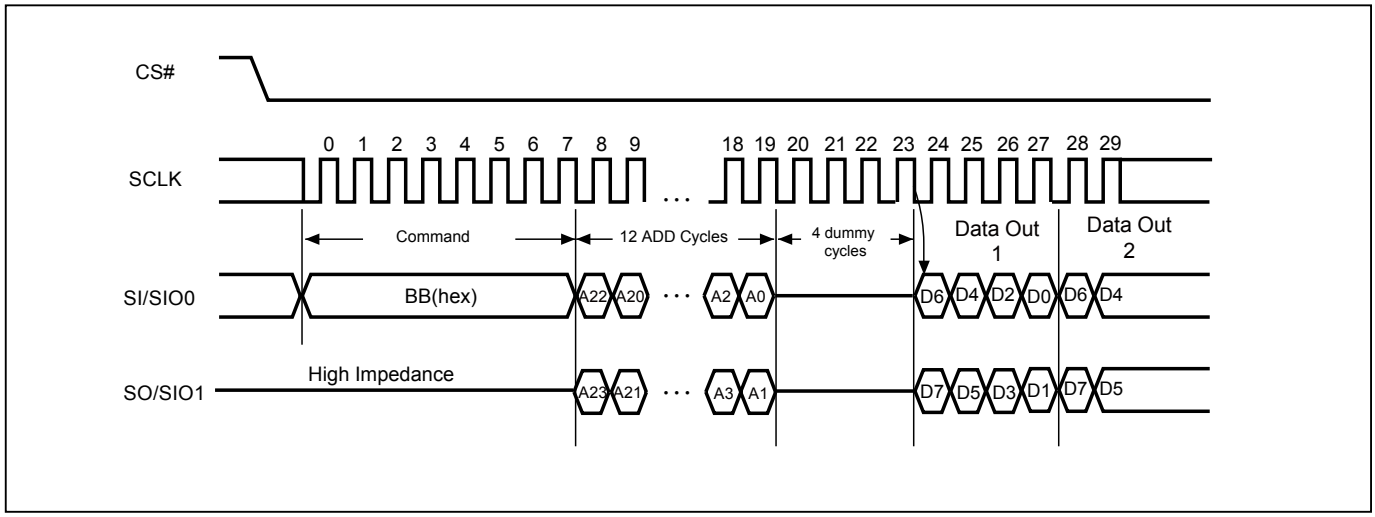
9-12. 2 x I/O Read Mode (2READ)

The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ send 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 17. 2 x I/O Read Mode Sequence (Command BBh)



9-13. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *"Table 2. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

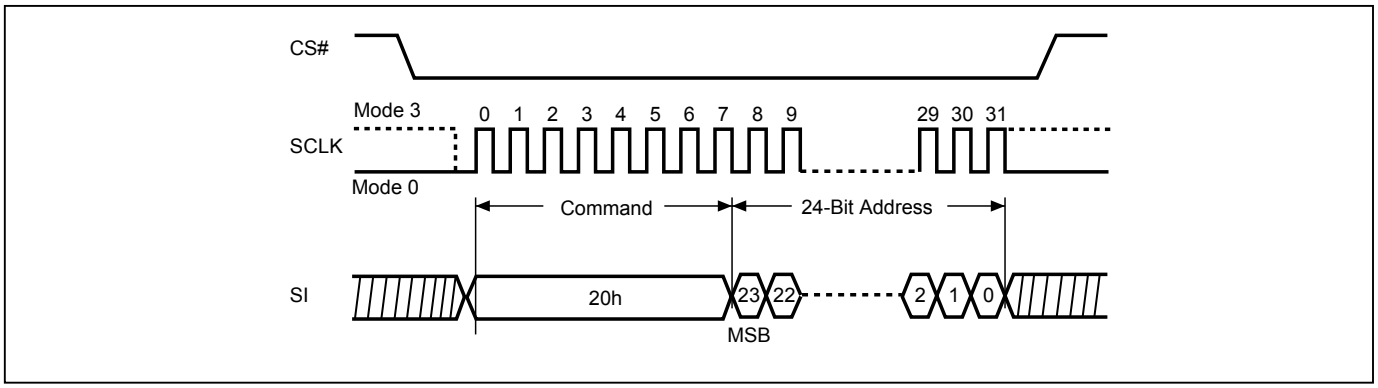
Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ send SE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[1:0] are "don't care".

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP0-BP3 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Figure 18. Sector Erase (SE) Sequence



9-14. Block Erase (BE32K)

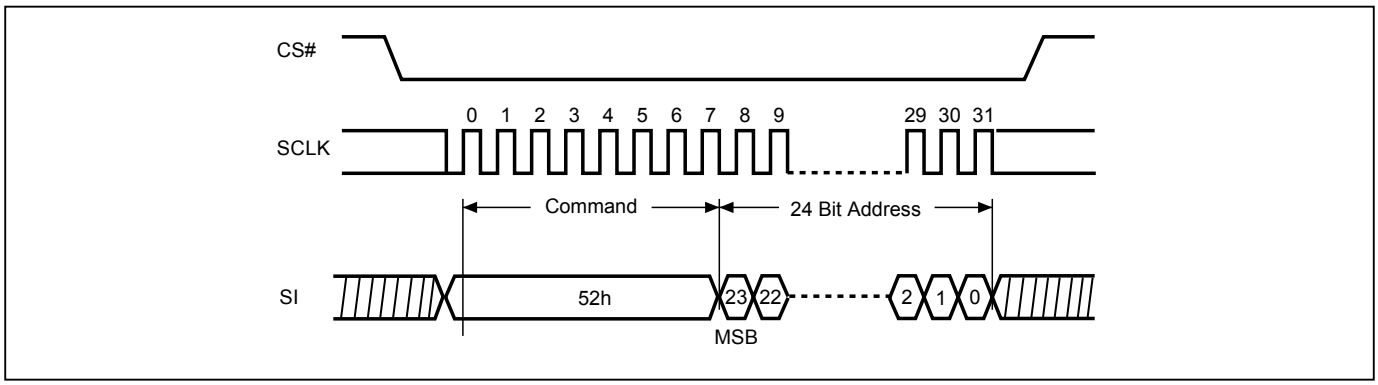
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (Please refer to *"Table 2. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → send BE32K instruction code → 3-byte address on SI → CS# goes high.

The SIO[1:0] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP0-BP3 bits, the array data will be protected (no change) and the WEL bit still be reset.

Figure 19. Block Erase 32KB (BE32K) Sequence (Command 52h)



9-15. Block Erase (BE)

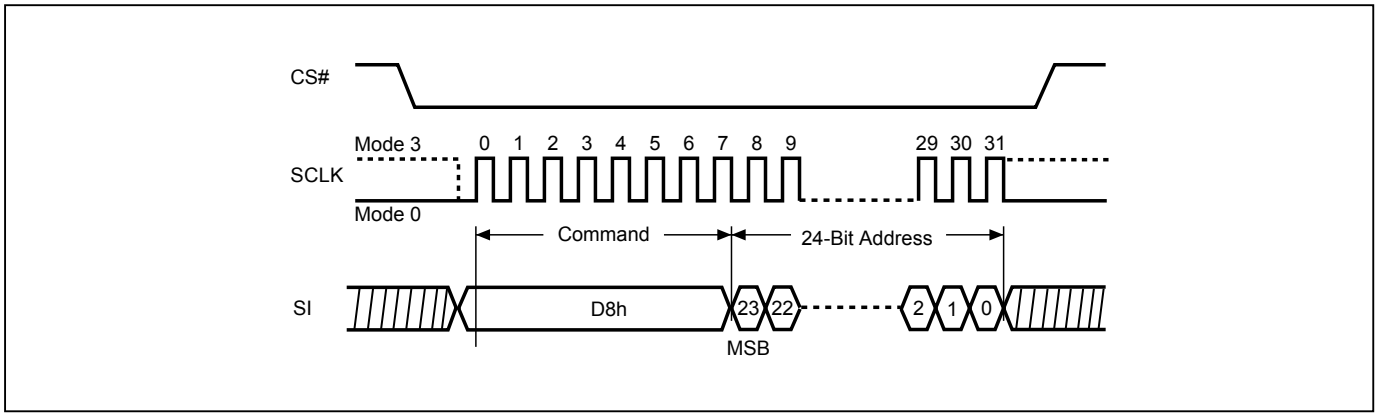
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 2. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ send BE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[1:0] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP0-BP3 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 20. Block Erase (BE) Sequence



9-16. Chip Erase (CE)

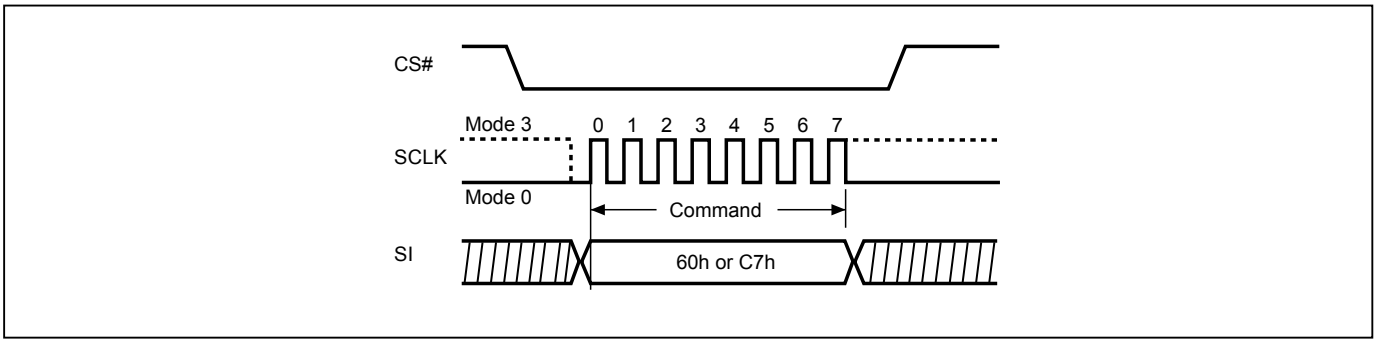
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→send CE instruction code→CS# goes high.

The SIO[1:0] are "don't care".

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP0-BP3 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP0-BP3 bits are all set to "0" or BP3, BP2, BP1, BP0 are set to "1,X,0,0".

Figure 21. Chip Erase (CE) Sequence



9-17. Page Program (PP)

The Page Program (PP) instruction is for programming memory bits to "0". One to 256 bytes can be sent to the device to be programmed. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If more than 256 data bytes are sent to the device, only the last 256 data bytes will be accepted and the previous data bytes will be disregarded. The Page Program instruction requires that all the data bytes fall within the same 256-byte page. The low order address byte A[7:0] specifies the starting address within the selected page. Bytes that will cross a page boundary will wrap to the beginning of the selected page. The device can accept (256 minus A[7:0]) data bytes without wrapping. If 256 data bytes are going to be programmed, A[7:0] should be set to 0.

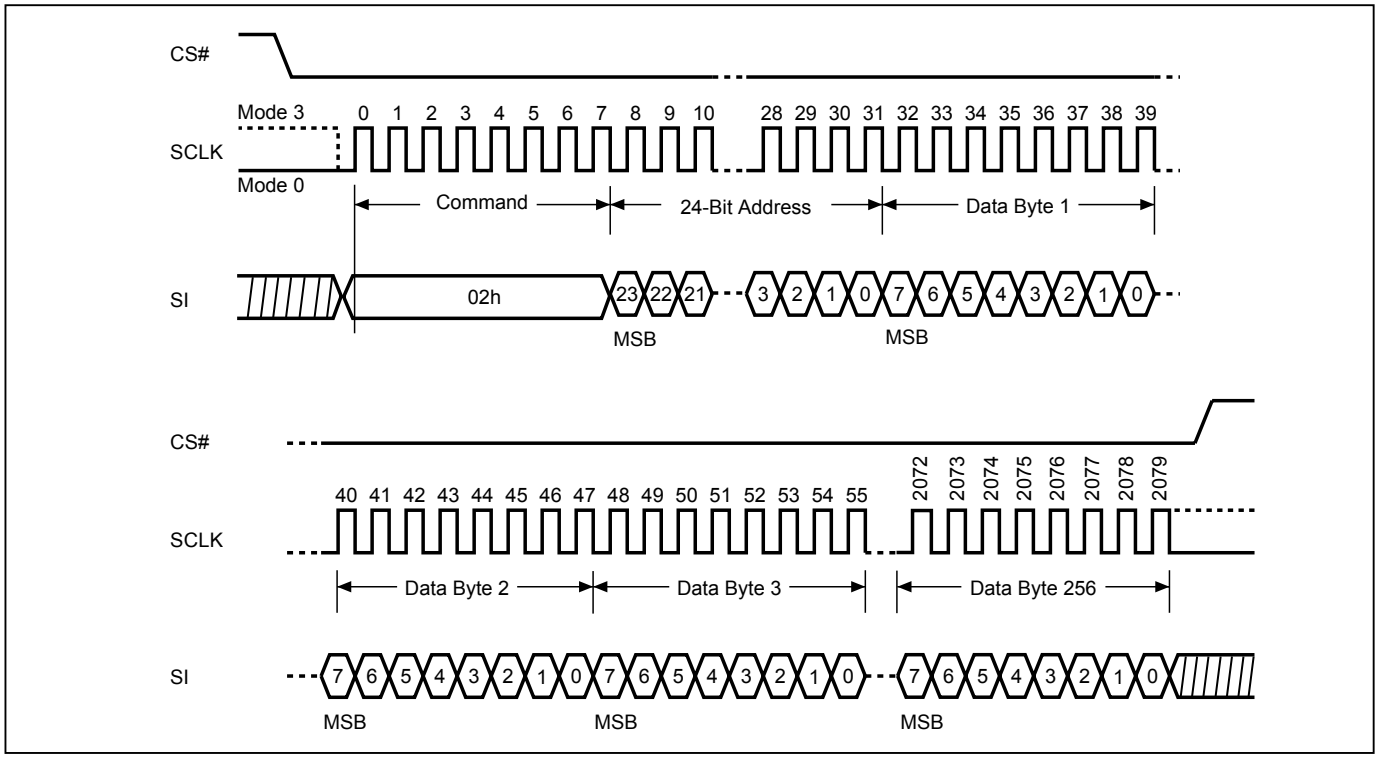
The sequence of issuing PP instruction is: CS# goes low→ send PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP0-BP3 bits, the Page Program (PP) instruction will not be executed.

The SIO[1:0] are "don't care".

Figure 22. Page Program (PP) Sequence



9-18. Deep Power-down (DP)

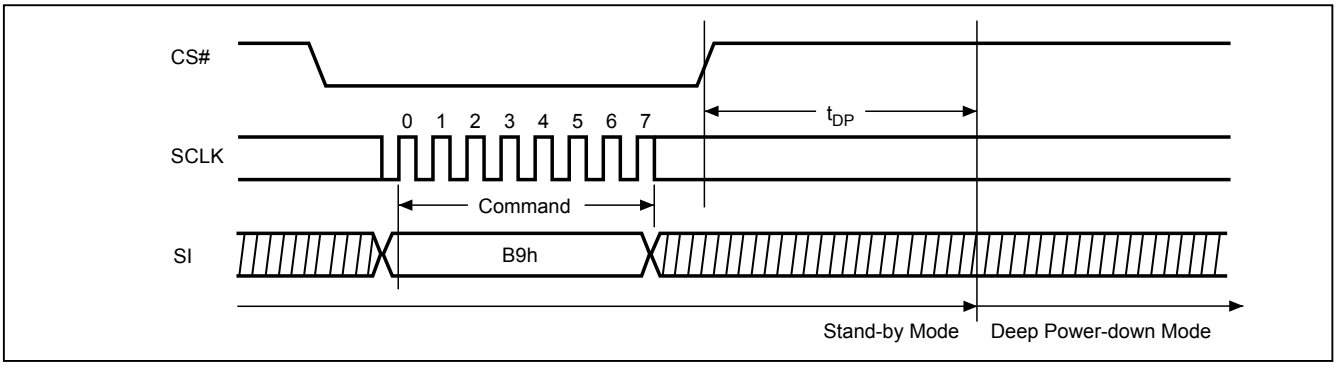
The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Powerdown mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Power-down (RDP) instruction, power-cycle, or reset. Please refer to *"Figure 25. Release from Deep Power-down (RDP) Sequence"*.

Figure 23. Deep Power-down (DP) Sequence (Command B9h)



9-19. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max). Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 4. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress.

The SIO[1:0] are don't care when during this mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

Figure 24. Read Electronic Signature (RES) Sequence (Command ABh)

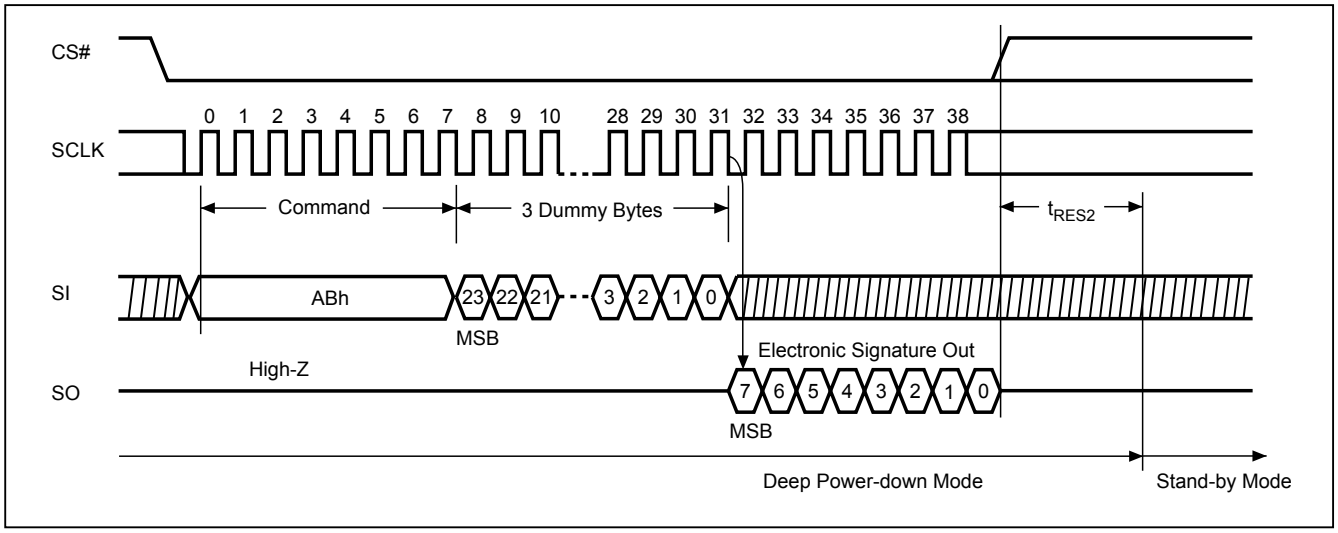
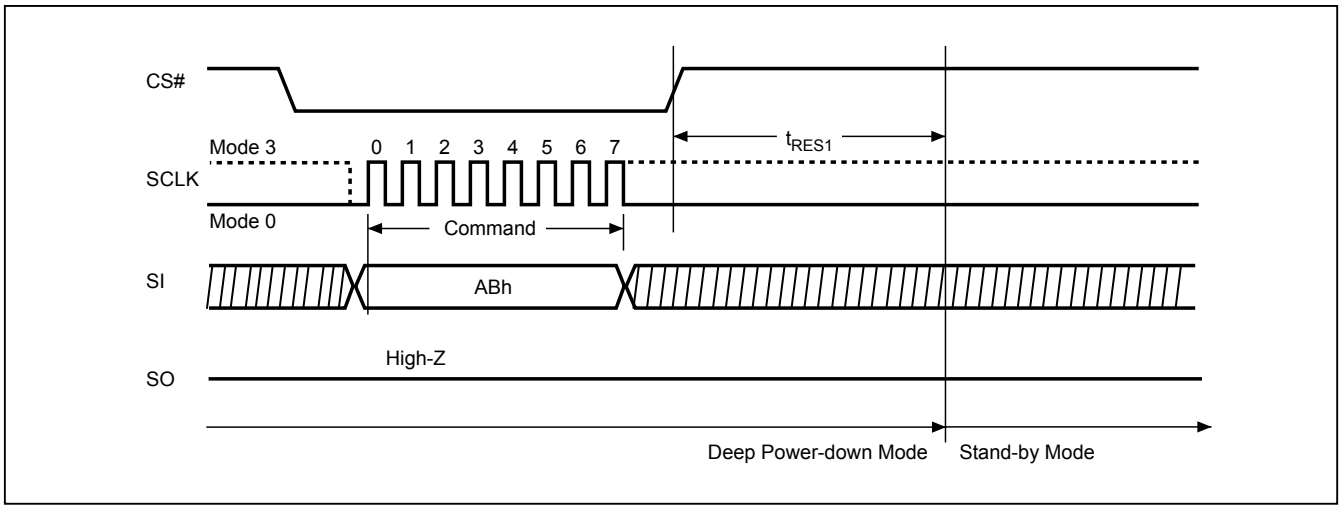


Figure 25. Release from Deep Power-down (RDP) Sequence



9-20. Software Reset - Reset-Enable (RSTEN) and Reset (RST)

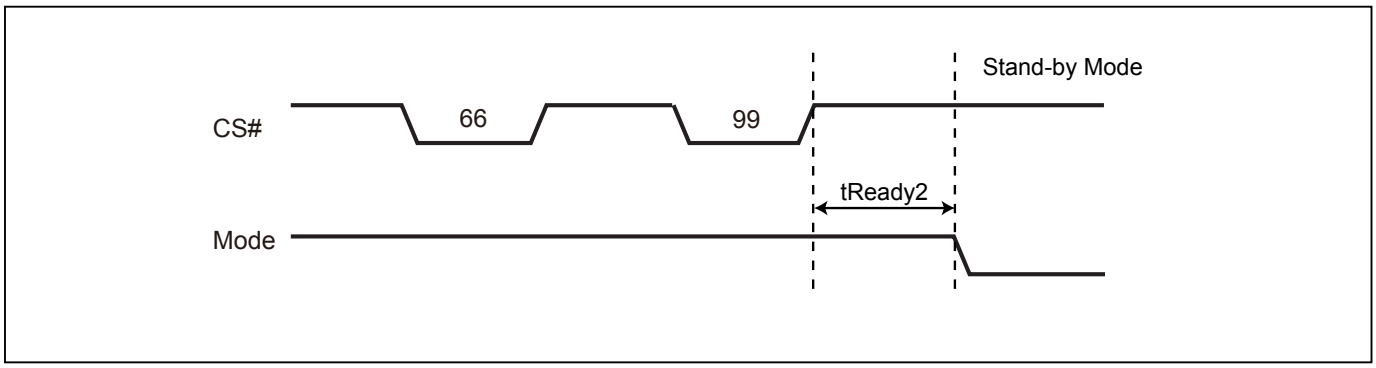
The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

Figure 26. Software Reset Recovery



10. POWER-ON STATE

The device is at the following states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the *"Figure 34. Power-up Timing".*

Notes:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Applied Input Voltage	-0.5V to VCC+0.5V
Applied Output Voltage	-0.5V to VCC+0.5V
VCC to Ground Potential	-0.5V to 4.0V

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V to VCC or -0.5V to GND for period up to 20ns.

Figure 27. Maximum Negative Overshoot Waveform

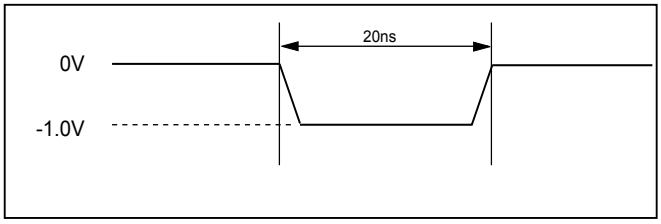
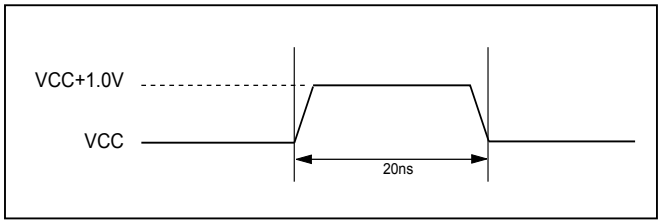


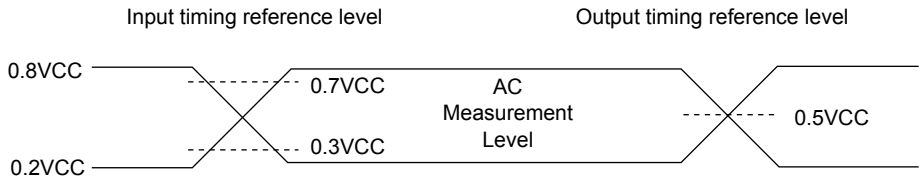
Figure 28. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

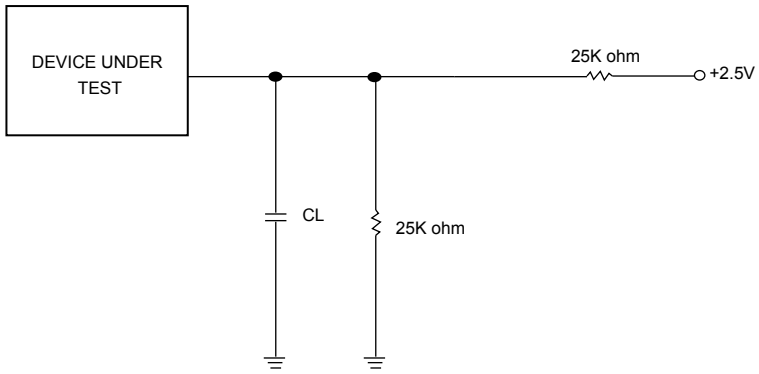
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 29. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are <5ns

Figure 30. OUTPUT LOADING



CL=30pF or 15pF Including jig capacitance

Figure 31. SCLK TIMING DEFINITION

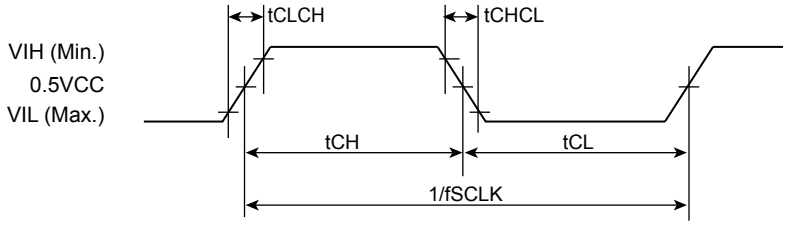


Table 7. DC CHARACTERISTICS

(Temperature = -40°C to 85°C for Industrial grade, VCC = 2.3V - 3.6V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1		± 0.02	± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1		± 0.02	± 2	uA	VCC = VCC Max VOUT = VCC or GND
ISB1	VCC Standby Current	1		5	25	uA	VIN = VCC or GND CS#=VCC
ISB2	Deep Power-down Current			1	10	uA	VIN = VCC or GND CS#=VCC
ICC1	VCC Read	1			6	mA	f=50MHz SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		5	20	mA	Program in Progress CS#=VCC
ICC3	VCC Write Status Register (WRSR) Current			2.1	15	mA	Program status register in progress CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		5	15	mA	Erase in Progress CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		5	20	mA	Erase in Progress CS#=VCC
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA
VWI	Low VCC Write Inhibit Voltage	3	1.5		2.1	V	

Notes :

1. *Typical values at VCC = 2.5V, T = 25°C. These currents are valid for all product versions (package and speeds).*
2. *Typical value is calculated by simulation.*
3. *Not 100% tested.*

Table 8. AC CHARACTERISTICS

(Temperature = -40°C to 85°C for Industrial grade, VCC = 2.3V - 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.(6)	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR		DC		80 (2.7-3.6V) 50 (2.3-2.7V)	MHz
fRSCLK	fR	Clock Frequency for READ instructions		DC		33	MHz
fTSCLK	fT	Clock Frequency for DREAD/2READ instructions		DC		80 (2.7-3.6V) 50 (2.3-2.7V)	MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK)	45%x (1/fSCLK)			ns
			Normal Read (fRSCLK)	13			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK)	45%x (1/fSCLK)			ns
			Normal Read (fRSCLK)	13			ns
tCLCH(2)		Clock Rise Time(3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time(3) (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		7			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		7			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		7			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		7			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read	20			ns
			From Write/Erase/Program to Read Status Register	40			ns
tSHQZ(2)	tDIS	Output Disable Time				6	ns
tCLQV	tV	Clock Low to Output Valid	Loading: 30pF			8	ns
			Loading: 15pF			6	ns
tCLQX	tHO	Output Hold Time		0			ns
tWHSL(4)		Write Protect Setup Time		20			ns
tSHWL(4)		Write Protect Hold Time		100			ns
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				8.8	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read				8.8	us
tW		Write Status Register Cycle Time			5	20	ms
tBP		Byte-Program			20	50	us
tPP		Page Program Cycle Time			1.6	10	ms
tSE		Sector Erase Cycle Time			50	500	ms
tBE32		Block Erase (32KB) Cycle Time			0.3	3.8	s
tBE(7)		Block Erase (64KB) Cycle Time			0.6	4	s
tCE(7)		Chip Erase Cycle Time			1.8	6.8	s
tREADY2		Reset Recovery time (During instruction decoding)		30			us
		Reset Recovery time (for read operation)		30			us
		Reset Recovery time (for program operation)		80			us
		Reset Recovery time(for SE4KB operation)		12			ms
		Reset Recovery time (for BE32KB/64KB operation)		12			ms
		Reset Recovery time (for Chip Erase operation)		12			ms
		Reset Recovery time (for WRSR operation)		0.1			ms

Notes:

1. *tCH + tCL must be greater than or equal to 1/f (fC or fR).*
2. *Value guaranteed by characterization, not 100% tested in production.*
3. *Expressed as a slew-rate.*
4. *Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.*
5. *Test condition is shown as "Figure 29. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL" and "Figure 30. OUTPUT LOADING".*
6. *Typical values given for TA=25°C. Not 100% tested.*
7. *The typical specification of tBE and tCE could be accelerated to 25ms and 50ms respectively when the 64KB block is blank (All FFh).*

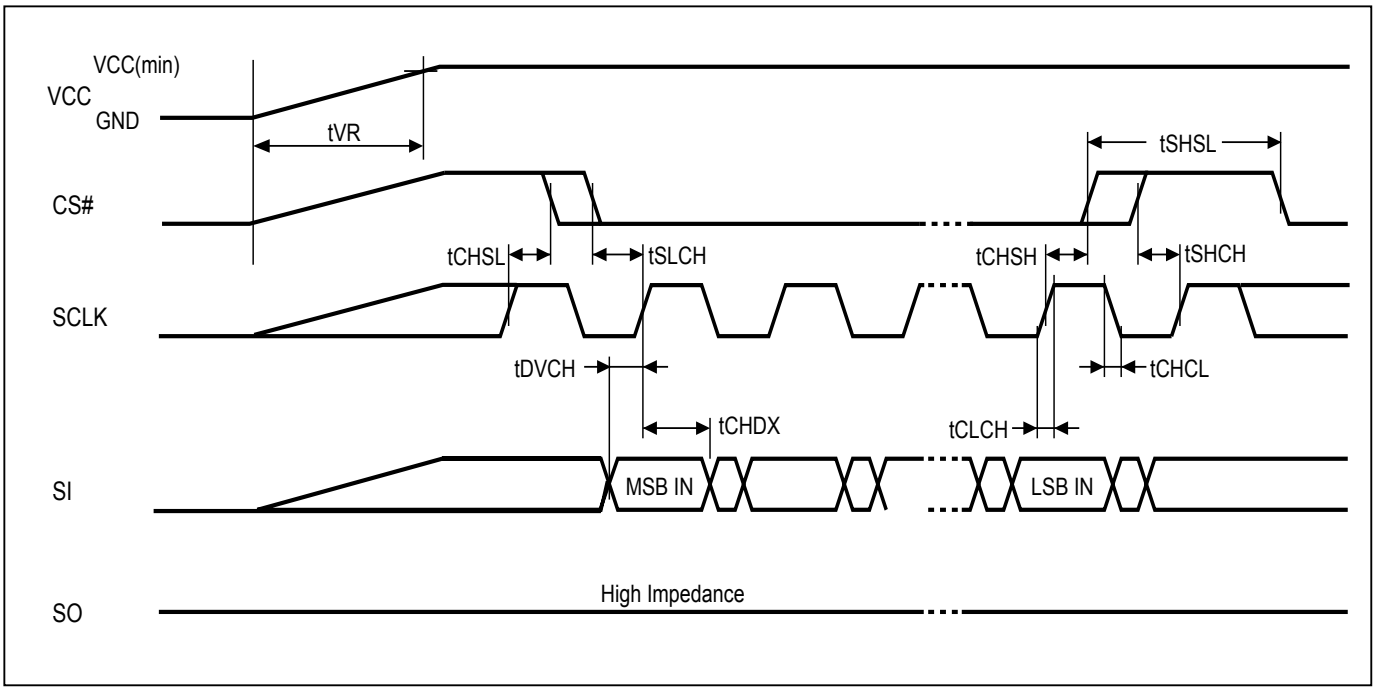
12. RECOMMENDED OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 32. AC Timing at Device Power-Up"* and *"Figure 33. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 32. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes :

1. Sampled, not 100% tested.

2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "Table 8. AC CHARACTERISTICS".

Figure 33. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

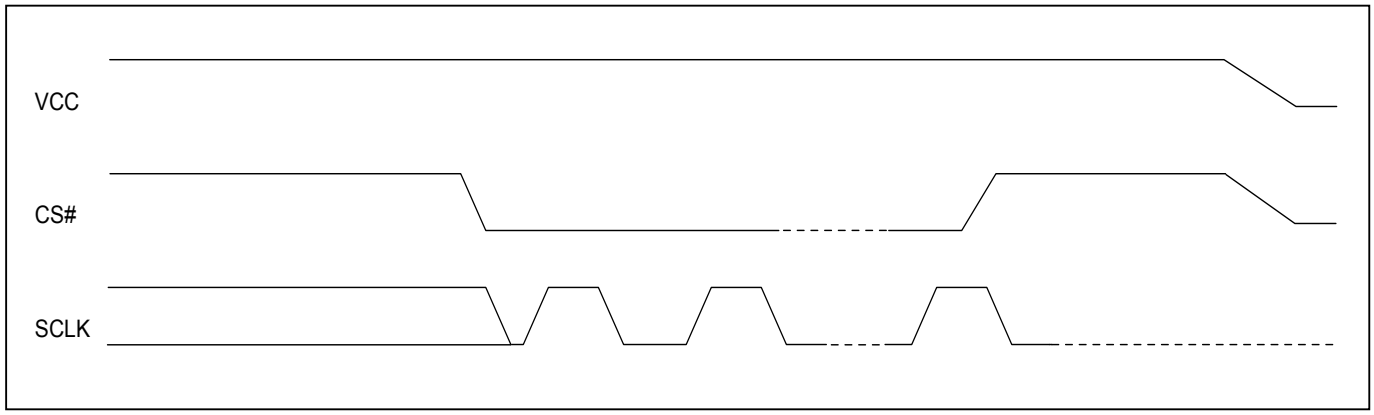


Figure 34. Power-up Timing

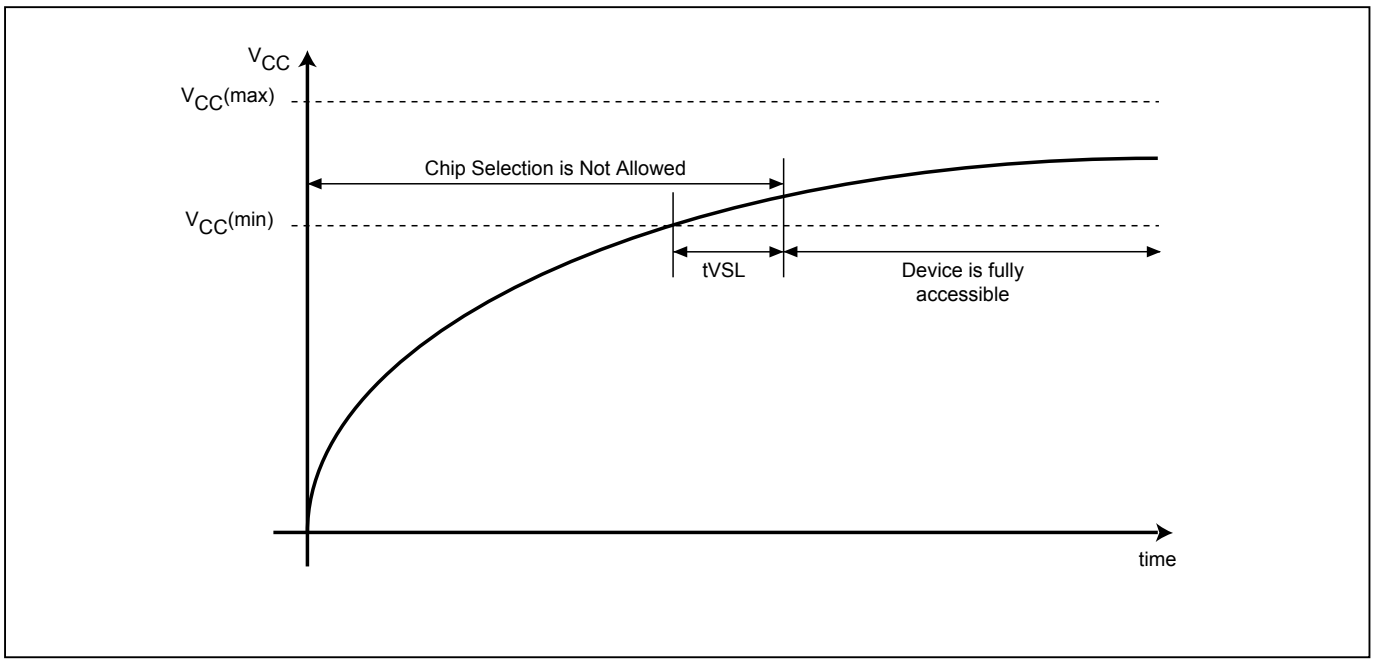


Figure 35. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below V_{PWD} for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 35. Power Up/Down and Voltage Drop"* and *"Table 9. Power-Up/Down Voltage and Timing"* below for more details.

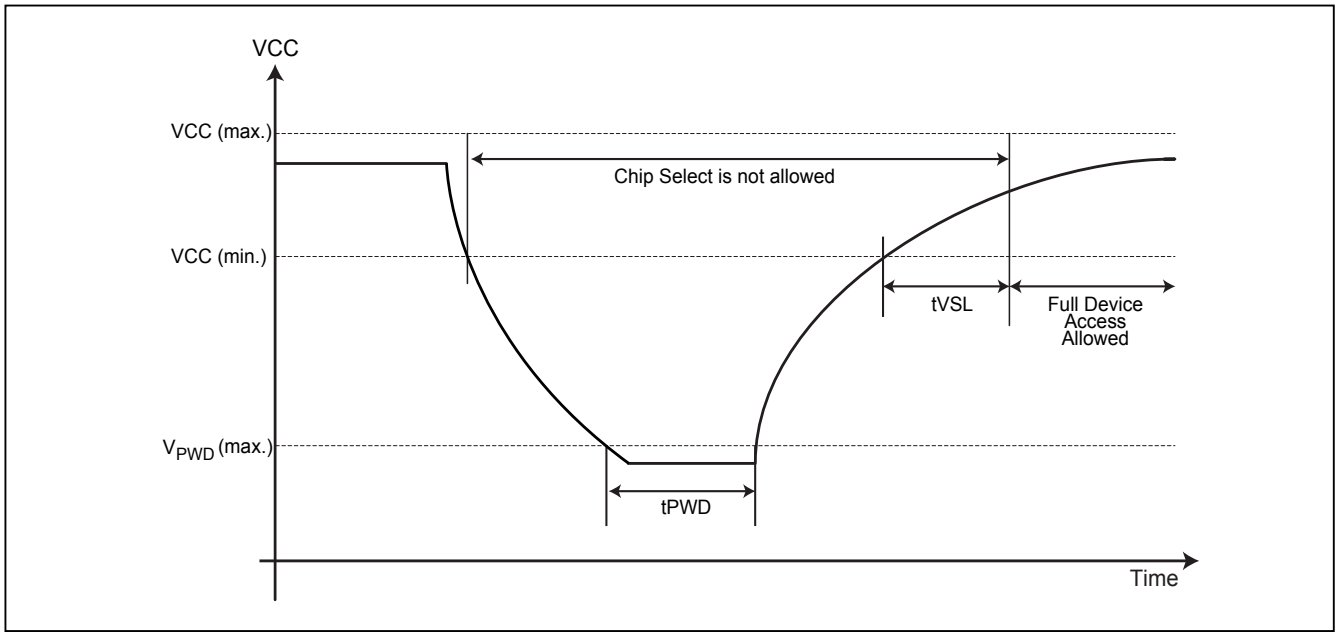


Table 9. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	800		us
VWI	Write Inhibit Voltage	1.5	2.1	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us

Note: *These parameters are characterized only.*

12-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

13. ERASE AND PROGRAMMING PERFORMANCE (2.3V - 3.6V)

Parameter	Min.	Typ.(1)	Max.(2)	Unit
Write Status Register Cycle Time		5	20	ms
Sector erase Time		50	500	ms
Block erase Time (tBE32)		0.3	3.8	s
Block erase Time (tBE)		0.6(5)	4	s
Chip Erase Time		1.8(5)	6.8	s
Byte Program Time (via page program command)		20	50	us
Page Program Time		1.6	10	ms
Erase/Program Cycle	100,000			cycles

Notes:

1. *Typical program and erase time assumes the following conditions: 25°C, 2.5V, and checkerboard pattern.*
2. *Under worst conditions of 85°C and 2.3V.*
3. *System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.*
4. *Erase/Program cycles comply with JEDEC: JESD47 & JESD22-A117 standard.*
5. *The typical specification of tBE and tCE could be accelerated to 25ms and 50ms respectively when the 64KB block is blank (All FFh).*

14. ERASE AND PROGRAMMING PERFORMANCE (Factory Mode)

Parameter	Min.	Typ.(1)	Max.(2)	Unit
Sector erase Time		20		ms
Block erase Time (tBE32)		0.16		s
Block erase Time (tBE)		0.35		s
Chip Erase Time		0.6		s
Page Program Time		1.3		ms
Erase/Program Cycle			50	cycles

Notice:

1. *Factory Mode must be operated in 20°C to 45°C and VCC 3.0V-3.6V.*
2. *In Factory mode, the Erase/Program operation should not exceed 50 cycles, and "ERASE AND PROGRAMMING PERFORMANCE" 100k cycles will not be affected.*

15. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

16. LATCH-UP CHARACTERISTICS

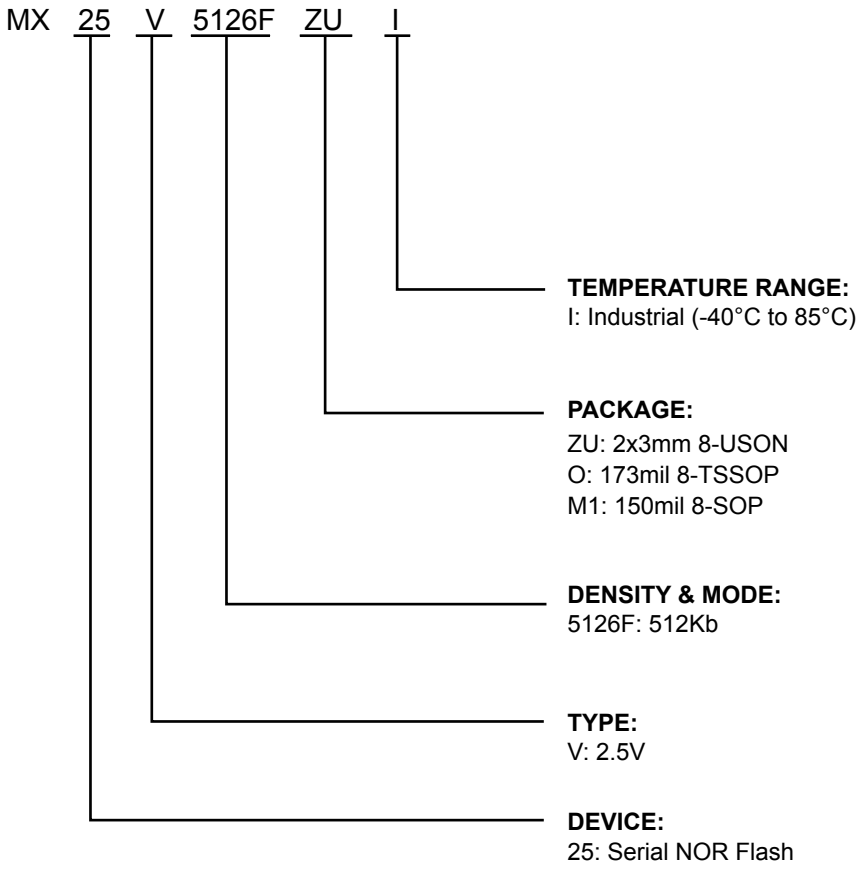
	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input Current on all non-power pins	-100mA	+100mA
Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JDESD78 standard).		

17. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	Voltage	Package	Temperature	Remark
MX25V5126FZUI	2.3V-3.6V	8-USON (2x3mm)	-40° to 85°C	
MX25V5126FOI	2.3V-3.6V	8-TSSOP (173mil)	-40° to 85°C	
MX25V5126FM1I	2.3V-3.6V	8-SOP (150mil)	-40° to 85°C	

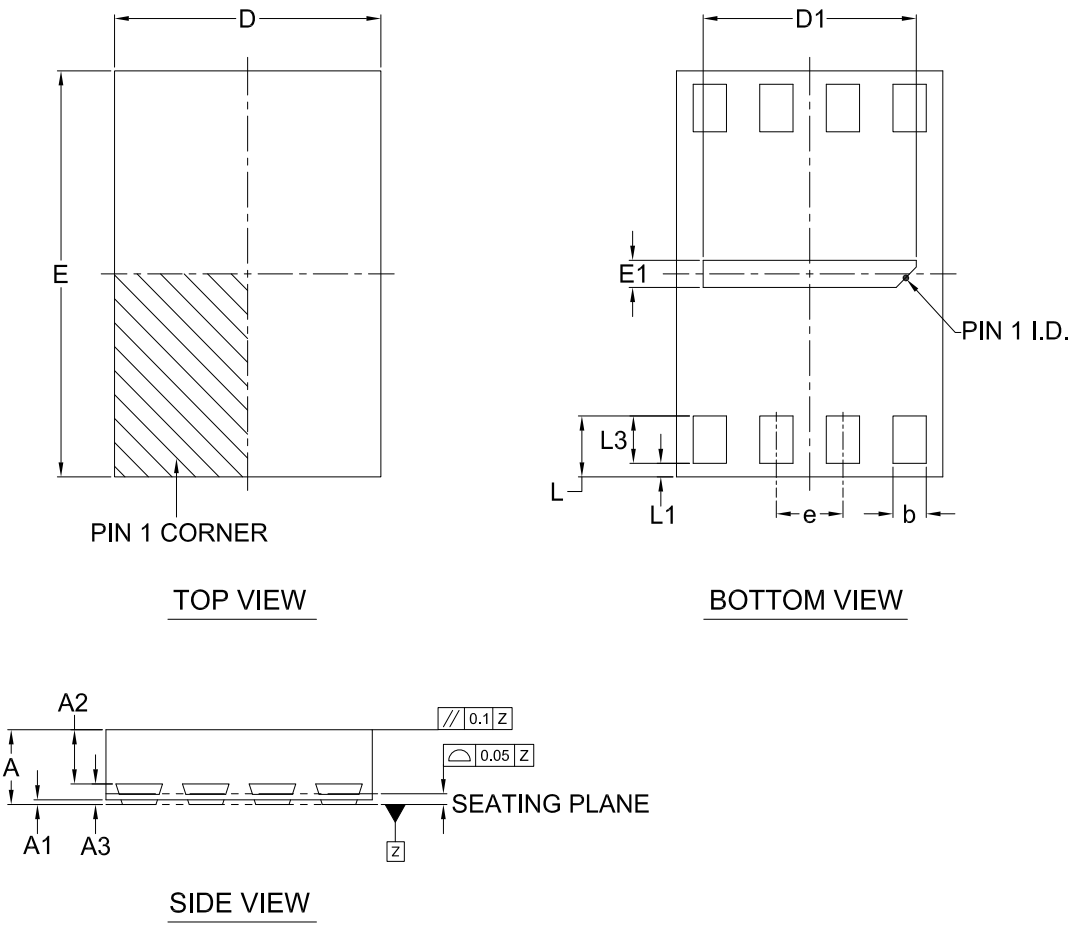
18. PART NAME DESCRIPTION



19. PACKAGE INFORMATION

19-1. 8-USON (2x3mm)

Doc. Title: Package Outline for USON 8L (2x3x0.6MM, LEAD PITCH 0.5MM)



Note:

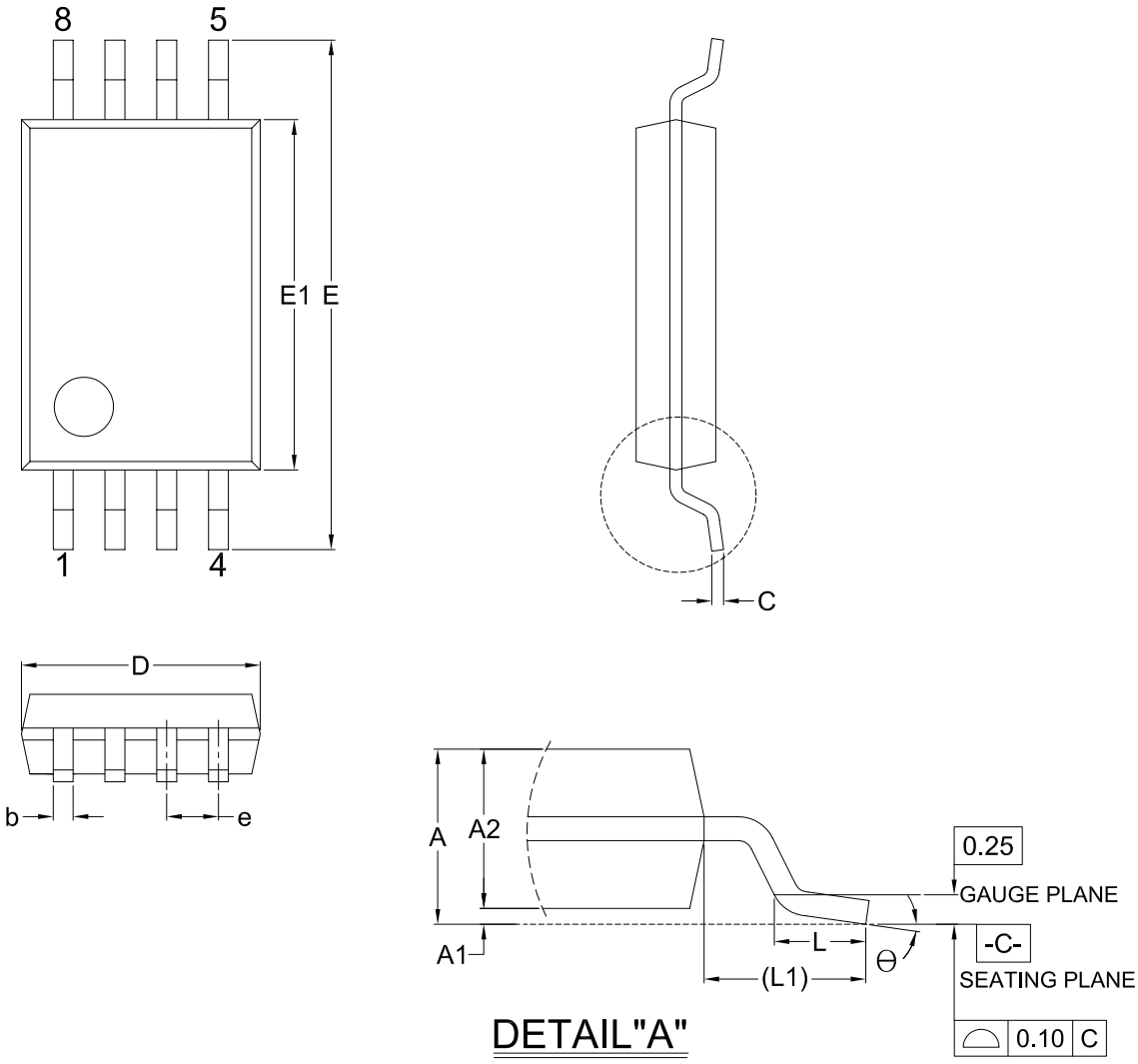
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	A3	b	D	D1	E	E1	e	L	L1	L3
mm	Min.	0.50	0	---	---	0.20	1.90	1.50	2.90	0.10	---	0.40	0	0.30
	Nom.	0.55	0.035	0.40	0.152	0.25	2.00	1.60	3.00	0.20	0.50	0.45	---	0.40
	Max.	0.60	0.05	0.425	---	0.30	2.10	1.70	3.10	0.30	---	0.50	0.15	0.50
Inch	MIn.	0.020	0	---	---	0.008	0.075	0.059	0.114	0.004	---	0.016	0	0.012
	Nom.	0.022	0.0014	0.016	0.0060	0.010	0.079	0.063	0.118	0.008	0.020	0.018	---	0.016
	Max.	0.024	0.002	0.0167	---	0.012	0.083	0.067	0.122	0.012	---	0.020	0.006	0.020

19-2. 8-pin TSSOP (173mil)

Doe. Title: Package Outline for TSSOP 8L (173MIL)

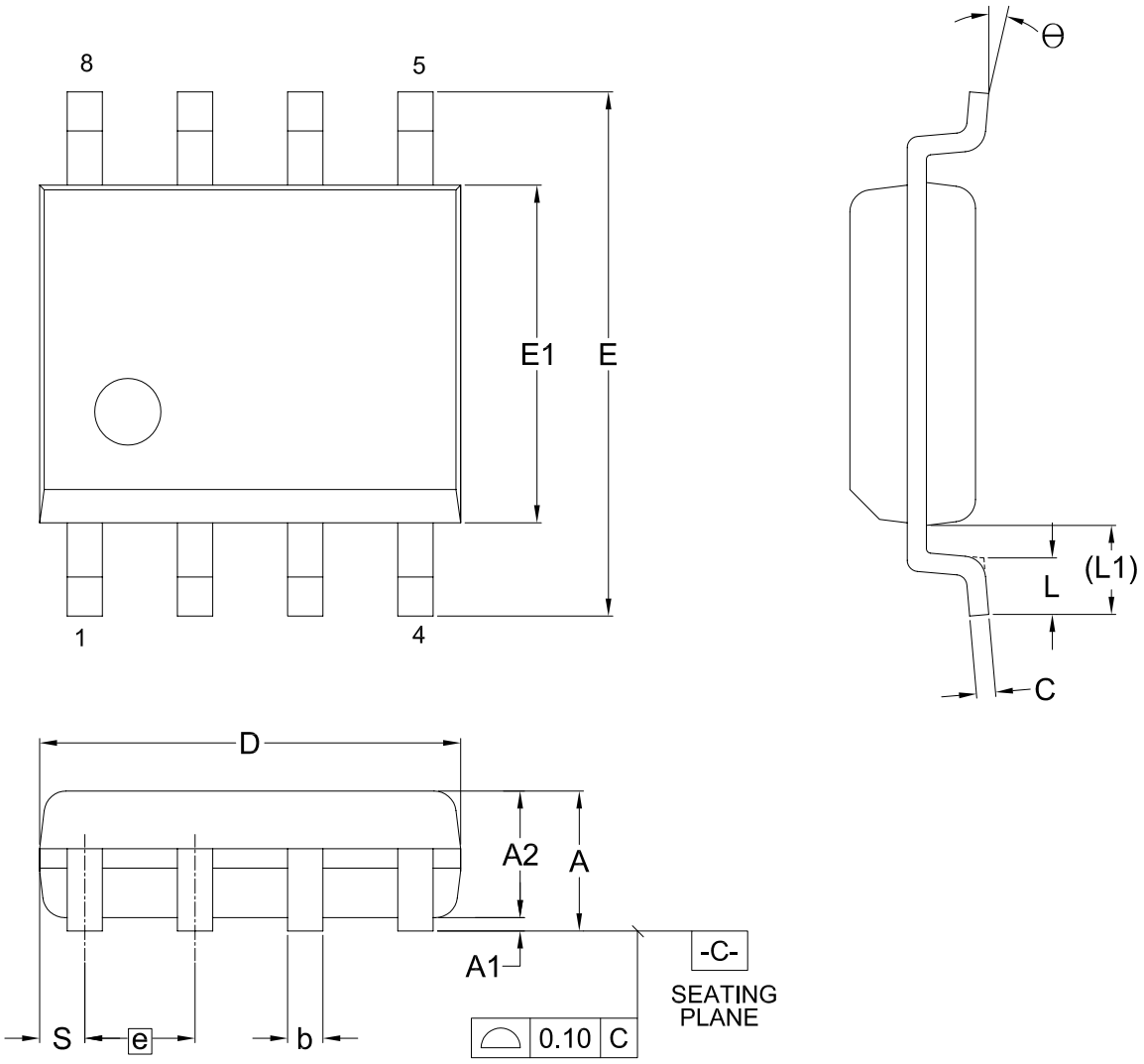


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	Θ
mm	Min.	--	0.05	0.80	0.20	0.10	2.90	6.30	4.30	—	0.45	0.85	0°
	Nom.	—	0.10	0.90	0.25	0.15	3.00	6.40	4.40	0.65	0.60	1.00	4°
	Max.	1.20	0.15	1.00	0.30	0.20	3.10	6.50	4.50	—	0.75	1.15	8°
Inch	Mln.	—	0.002	0.031	0.008	0.004	0.114	0.248	0.169	--	0.018	0.033	0°
	Nom.	—	0.004	0.035	0.010	0.006	0.118	0.252	0.173	0.026	0.024	0.039	4°
	Max.	0.047	0.006	0.039	0.012	0.008	0.122	0.256	0.177	--	0.030	0.045	8°

19-3. 8-pin SOP (150mil)

Doe. Title: Package Outline for SOP 8L (150MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80	---	0.46	0.85	0.41	0°
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5°
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	---	0.86	1.25	0.67	8°
Inch	MIn.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150	---	0.018	0.033	0.016	0°
	Nom.	---	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5°
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	---	0.034	0.049	0.026	8°

20. REVISION HISTORY

Revision	Descriptions	Page
June 01, 2018		
0.00	1. Initial Release.	All
July 09, 2019		
1.0	1. Removed "Advanced Information" to align with the product status.	All
	2. Revised *"Figure 17. 2 x I/O Read Mode Sequence (Command BBh)"*.	P29
	3. Updated the title of Figure 29.	P41
	4. Revised LATCH-UP testing descriptions.	P48

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